Interface Charge Sensitivity and Short-Channel Effect Mitigation in Asymmetrical Source Step-Channel FinFETs

Palle Rangappa, Anchula Sathish

Abstract—**In the rapidly evolving landscape of the VLSI industry, the quest for further miniaturization of electronic devices has driven the development of nanoscale transistors, with traditional MOSFETs struggling to meet the performance demands due to pronounced short-channel effects. These effects, such as drain-induced barrier lowering (DIBL), gate oxide leakage, and mobility degradation, significantly hinder the scaling potential of conventional CMOS technology. To address these challenges, this study explores the Step Channel Double Gate FinFET (SC-FinFET) architecture, with a focus on a novel Asymmetrical Source configuration (ASSC-FinFET), compared to the conventional Symmetrical Source design (SSSC-FinFET). In comparison, the traditional SSSC-FinFET demonstrated higher sensitivity to interface charges, leading to greater variability in electron concentration and lateral electric field distribution. This variability could introduce instability in device performance under different operating conditions, making the ASSC-FinFET a more robust alternative for future applications. The study concludes that the ASSC-FinFET not only addresses the limitations of conventional MOSFETs but also offers a scalable and reliable solution for the next generation of high-performance, energy-efficient electronic devices. As the semiconductor industry continues to demand smaller, faster, and more efficient components, the ASSC-FinFET stands out as a promising candidate to meet these challenges, potentially driving significant advancements in computing technology.**

Index Terms—**FinFET, Asymmetrical source, electric field, high performance, energy efficient**

I. Introduction

THE relentless pursuit of miniaturization in the VLSI industry has led to the development of nanoscale transistors, pushing the boundaries of fabrication technology and materials science [1]. While MOSFETs have been the dominant device for decades, their performance has been constrained by short-channel effects as channel lengths have shrunk. These effects, such as drain-induced barrier lowering (DIBL), gate oxide leakage, and mobility degradation, can significantly degrade device performance and limit the scaling potential of traditional CMOS technology [2].

To address these challenges, researchers have explored innovative device architectures that can deliver high currents, low power consumption, and improved subthreshold swing. These advancements are crucial for enabling future generations of high-performance [3], energy-efficient computing systems. Some promising candidates include FinFETs, GAAFETs, and TFETs, each offering unique advantages in terms of device performance and scalability [4]. By overcoming the limitations of traditional MOSFETs, these new device architectures have the potential to revolutionize the semiconductor industry and drive further advancements in computing technology [5].

The step channel FinFET is a three-dimensional field-effect transistor (FET) designed to overcome the limitations of traditional planar MOSFETs at nanoscale dimensions [6,7,8]. Its unique structure, featuring a fin-shaped channel surrounded by a gate on multiple sides, provides several advantages, including improved channel control, reduced short-channel effects, and enhanced performance. The stepped shape of the channel not only optimizes space utilization but also minimizes parasitic capacitances, leading to improved device performance [9,10,11,12]. Additionally, the thicker oxide layer at the source and drain regions helps to suppress leakage currents, enhancing device reliability and reducing power consumption [13].

Compared to conventional MOSFETs, the step channel FinFET delivers higher drive currents and exhibits improved subthreshold swing [14,15]. This translates to better performance in terms of switching speed and power efficiency, making it a promising candidate for future high-performance integrated circuits. While the step channel FinFET has demonstrated significant advantages, it is important to note that its fabrication process can be more complex compared to traditional MOSFETs. However, the potential benefits in terms of performance and scalability make it a worthwhile investment for the semiconductor industry [16]. As technology continues to advance, the step channel FinFET is poised to play a crucial role in driving innovation and enabling the development of more powerful and energy-efficient electronic devices [17,18,19].

In recent years, there has been a growing body of literature exploring the design, fabrication, and characterization of step channel FinFETs. Researchers have investigated various design parameters, such as channel length, fin height, and gate dimensions, to optimize device performance and minimize short-channel effects. Fabrication techniques for step channel FinFETs have also been developed, building upon existing CMOS processes. These techniques involve complex lithography and etching steps to create the three-dimensional structure of the device. Numerous studies have demonstrated the superior performance of step channel FinFETs compared to traditional MOSFETs [20,21]. They have shown higher drive currents, improved subthreshold swing, and reduced leakage currents. Additionally, researchers have

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Palle Rangappa is a Research Scholar of Department of ECE, JNTUA, Anantapuramu, Andhra Pradesh, India. He is also an Assistant Professor of Department of ECE, Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal, Andhra Pradesh, India. (e-mail: palleranga.476@gmail.com).

Anchula Sathish is a Professor of Department of ECE, Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal, Andhra Pradesh, India. (e-mail: sathishanchula@gmail.com).

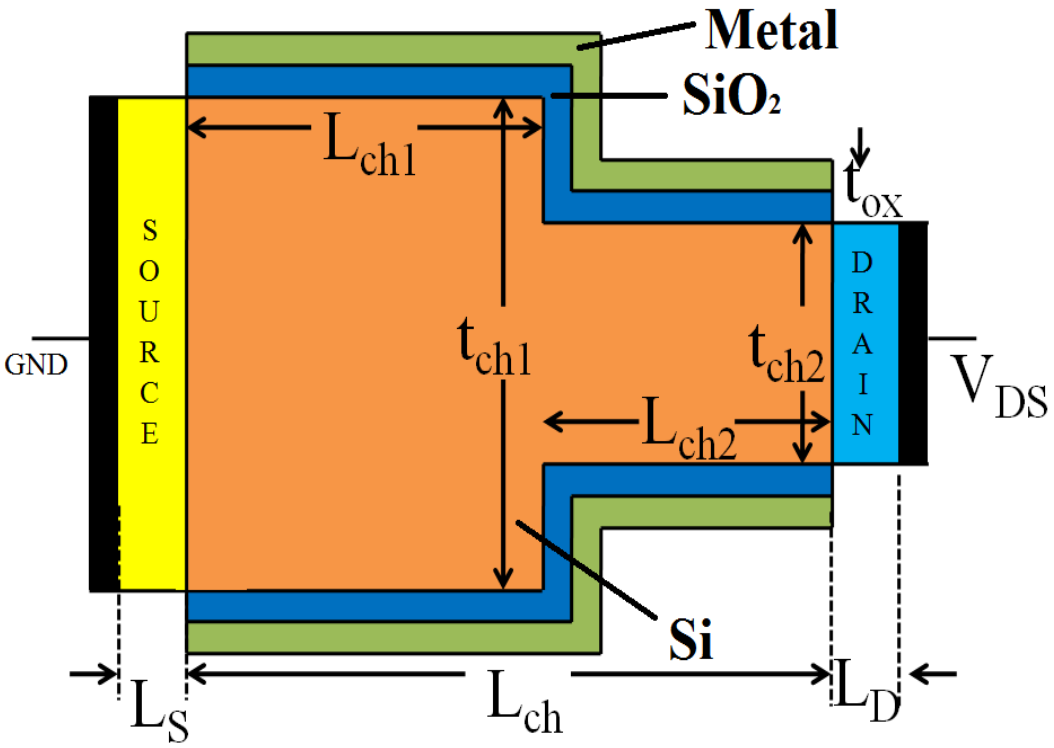


Fig. 1: Structure of Symmetrical Source Step Channel Double Gate FinFET (SSSC-FinFET)

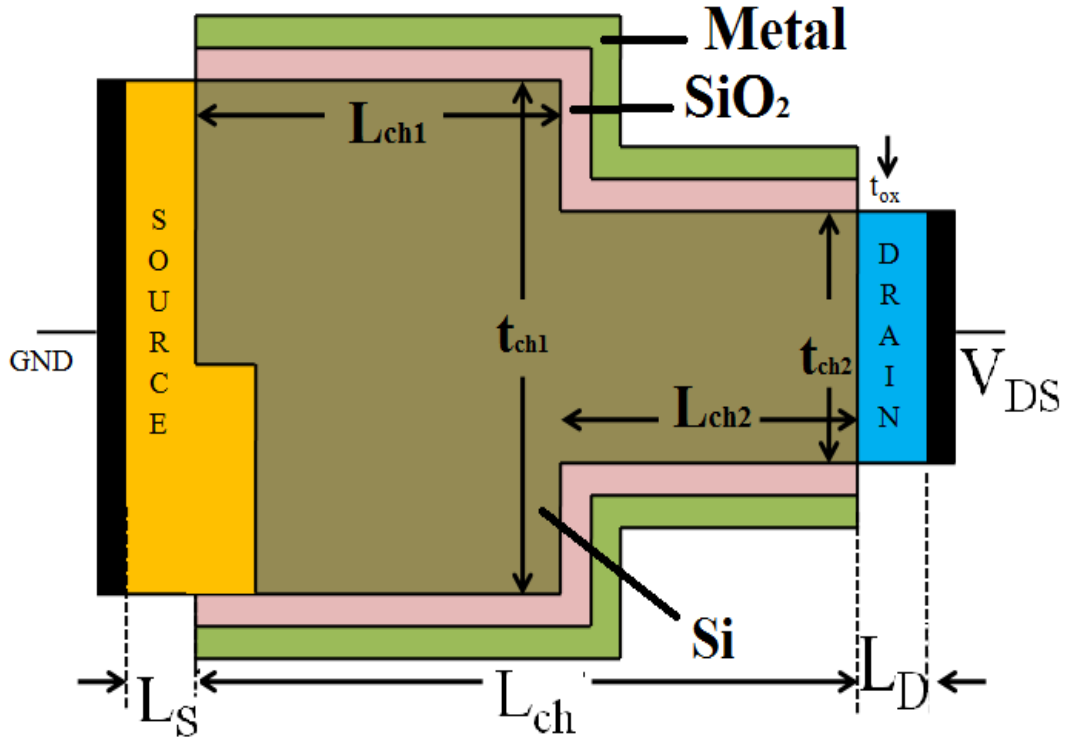


Fig. 2: Structure of Asymmetrical Source Step Channel Double Gate FinFET (ASSC-FinFET)

explored the use of different materials, such as high-mobility channel materials, to further enhance device performance [22]. While the step channel FinFET holds great promise, there are still challenges to be addressed. One area of ongoing research is the development of reliable and cost-effective fabrication processes. Additionally, the integration of step channel FinFETs into complex integrated circuits requires careful consideration of layout and design rules [23].

Despite these challenges, the step channel FinFET is a promising technology that has the potential to drive significant advancements in the semiconductor industry [24,25]. Its unique characteristics and superior performance make it a compelling candidate for future generations of electronic devices. As research and development continue, we can

TABLE I: Device dimensions and materials used in simulation

Parameter	Value	Units
Device Length (L_S+L_{ch}+L_D)	24	nm
Device Width	13	nm
Channel Length	18	nm
L_{ch1} Width	7	nm
L_{ch2} Width	1	nm
Channel material	Silicon	-
Doping concentration of L_{ch1}	1×10^{16}	cm^{-3}
Doping concentration of L_{ch2}	1×10^{16}	cm^{-3}
Source Doping concentration	2×10^{20}	cm^{-3}
Drain Doping concentration	2×10^{20}	cm^{-3}
Workfunction of Gate	4.6	eV

expect to see even more exciting applications and innovations based on this promising technology [26].

II. Strucutre Of Proposed Device

The depicted device in Figure.1 is a Symmetrical Source Step Channel Double Gate FinFET (SSSC-FinFET), a type of field-effect transistor (FET) designed to overcome the limitations of traditional planar MOSFETs at nanoscale dimensions. The device features a three-dimensional structure with a fin-shaped channel surrounded by a gate on multiple sides, providing enhanced control over the channel and reduced short-channel effects. Key dimensions include device length (L_{ch}), channel length (L_{ch1}, L_{ch2}), source/drain length (L_s, L_d), fin height (t_{ch1}, t_{ch2}), and gate oxide thickness (t_{ox}). The device's structure and materials contribute to its improved performance and scalability compared to traditional MOSFETs, making it a promising candidate for future high-performance electronic applications. Also, Figure.2 shows proposed Asymmetrical Source Step Channel Double Gate FinFET (ASSC-FinFET) with source extended to the channel.

Table 1 shows the device dimensions and materials used for the devices. The n-type doping in regions of source and drain with a high concentration of 2×10^{20} cm^{-3}. The p-type doping with a lower concentration of 1×10^{16} cm^{-3}, likely represents the channel region, where careful control of carrier concentration is necessary for the device operation. This doping profile indicates a device designed for unipolar conduction, likely a MOSFET, with distinct n-type and p-type regions. Various physical models to simulate the behavior of the device under various conditions are used. Models for carrier mobility, Shockley-Read-Hall (SRH) recombination, field-dependent mobility, and bandgap narrowing are included. These models are crucial for accurately capturing the complex interactions within the semiconductor material, especially under high electric fields or varying temperature conditions. The work function of the gate electrodes is also specified as 4.6 eV, ensuring that the electrostatic behavior of the device is correctly modeled.

III. Results & Discussion

In Figure 3, it is observed that SSSC-FinFET shows significant fluctuations in the drain current curves. It can be explicitly seen that the fluctuations are directly proportional to the sensitivity of the symmetrical source design to interface charges. For a higher gate voltage, electron concentration in the channel varies significantly and thus the existing fluctuations in the drain current become moderately significant. These characteristics suggest that the symmetrical source structure of the SSSCFinFET does not support robustness in sustaining stable current flow and is thus more vulnerable to performance fluctuations under changing interface charge conditions.

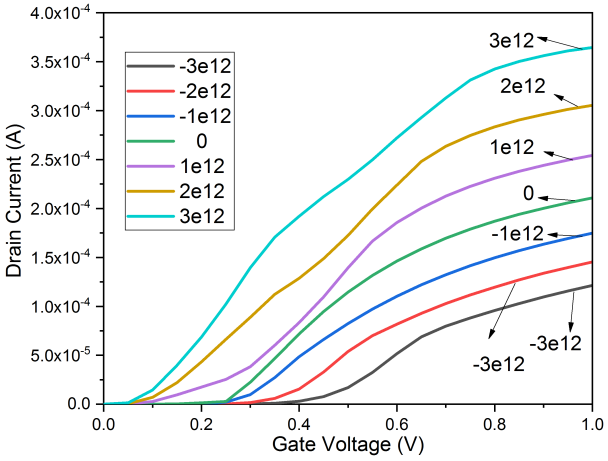


Fig. 3: Drain Current characteristics of SSSC-FinFET

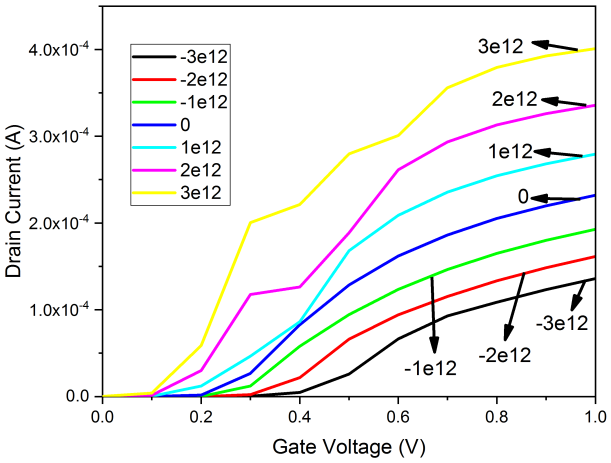


Fig. 4: Drain Current characteristics of ASSC-FinFET

On the other hand, figure 4 illustrates that the ASSC-FinFET has much less drain current variability with interface charge condition. This is due to the asymmetrical source design, in which the source extends into the channel region. A reduced sensitivity of the device to interface charges is thus realized, which consequently means that the curves are well grouped with gentle transitions, presenting better stability and predictability of the device's performance. Asymmetry improves electrostatic control in the channel, enabling a better modulation of carrier concentration with reduced short-channel effects.

Transconductance (g_m) is an essential parameter for the assessment of the performance of FET devices, characterized by the device's ability to control the output current through the applied gate voltage. The characteristic of these figures is depicted by the structural differences between the two topologies and their response to the concentration of electrons in the channel.

In Figure 5, transconductance of SSSC-FinFET exhibits

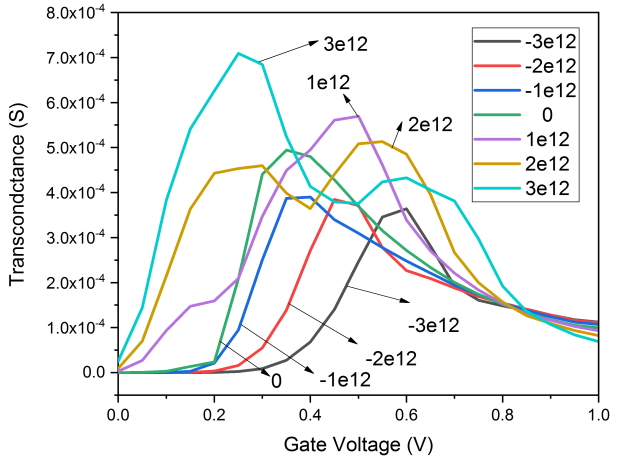


Fig. 5: Variation of Transconductance with Gate voltage for SSSC-FinFET

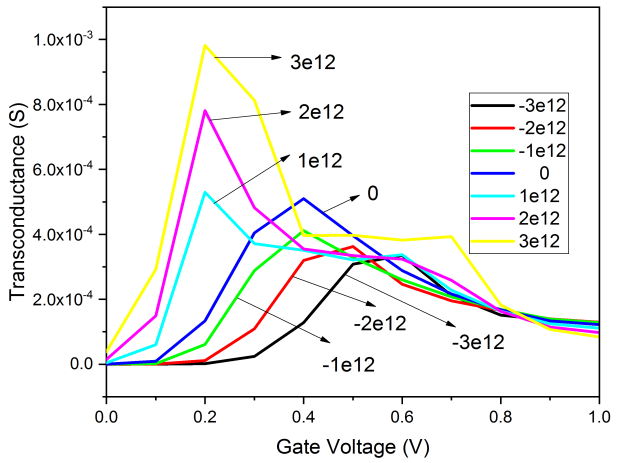


Fig. 6: Variation of Transconductance with Gate voltage for ASSC-FinFET

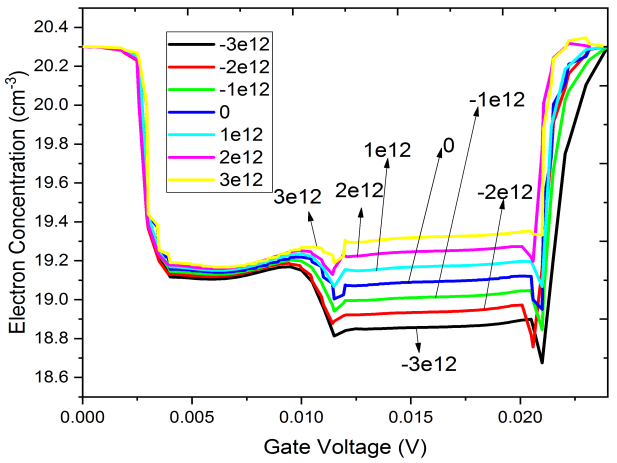


Fig. 7: Electron concentration distribution of SSSC-FinFET

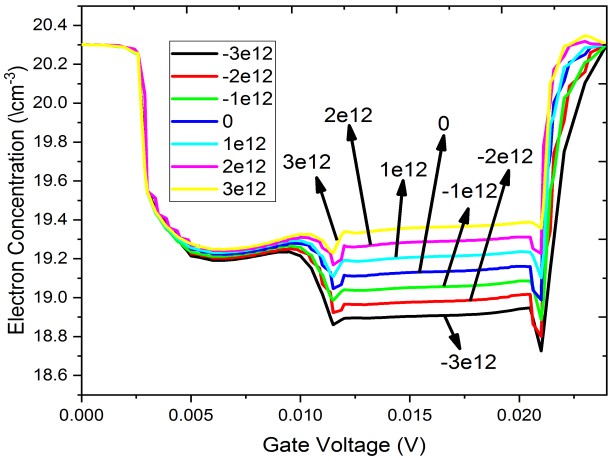


Fig. 8: Electron concentration distribution of ASSC-FinFET

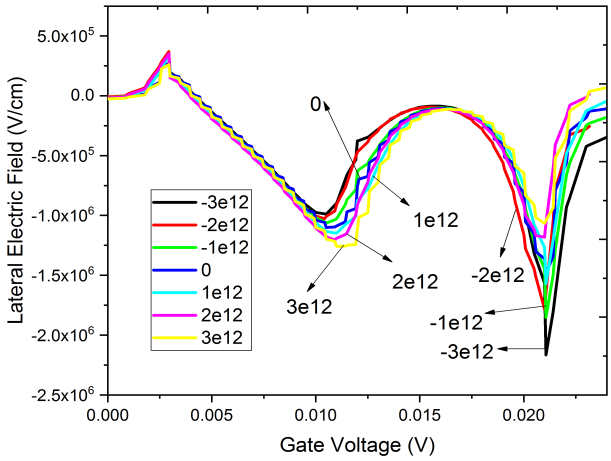


Fig. 9: Lateral Electric Field distribution of SSSC-FinFET

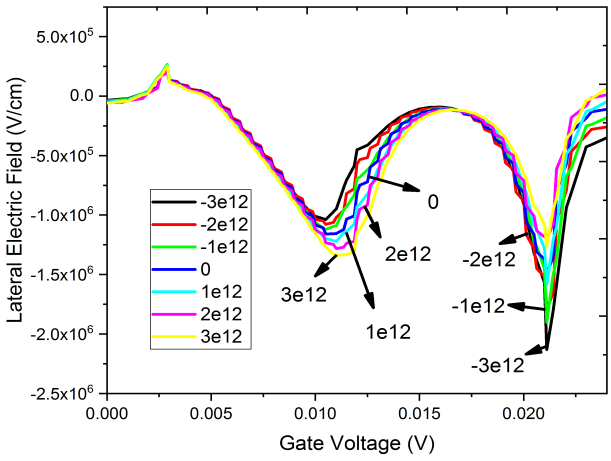


Fig. 10: Lateral Electric Field distribution of ASSC-FinFETe

highly fluctuating and widely peaking trends with gate voltage. Such features can be attributed to the source structure design being highly sensitive to interface charge variations. The asymmetrical structure naturally results in an uneven modulation of channel electron concentration upon gate voltage variation. This sets up a relation between current and gate voltage as irregularities in it. These irregularities occur as sudden spikes and troughs in the transconductance curve. This source structure that is not robust in its balanced design causes inconsistent behavior from the device, so the device cannot readily anticipate when it will behave inconsistently. The electric field inside the channel is highly non-uniform with a variation in concentration of charge at the interface; thus, there is irregular modulation of the carrier concentration

and mobility. Therefore, the peaks in the transconductance curves show an extreme sensitivity to the interface charge, and this capability of the device to control the current with the gate voltage very sensitively related to the interface charge induces instability and inconsistency in the performance of the device.

Figure 6 displays the transconductance curve obtained from the ASSC-FinFET, which is smoother and more stable. Introducing the asymmetrical source design introduces better control over the channel, allowing the electron concentration to be modulated more uniformly with the gate voltage. That uniformity again reduces abrupt changes in the current gate-voltage relationship, and this simplifies the variation of the transconductance. The reduced interface charge sensitivity in the ASSC FinFET has proved to be an important enabler for stabilizing these features. In addition, the extended source of the ASSC FinFET facilitates the optimization of the electric field distribution, allowing for efficient charge carrier injection into the channel and reduction of carrier scattering. The source extended creates a more gradual and controlled distribution of the electric field, which also reduces the effects of the charges from the interface on the channel. The phenomenon influencing the mobility and concentration of the carriers was now significantly damped whenever the concentration of the interface charge varies, hence exhibiting stable transconductance behavior. The closer grouping of curves illustrates that ASSC-FinFET can sustain consistent performance even when variances occur in the concentration of the interface charge.

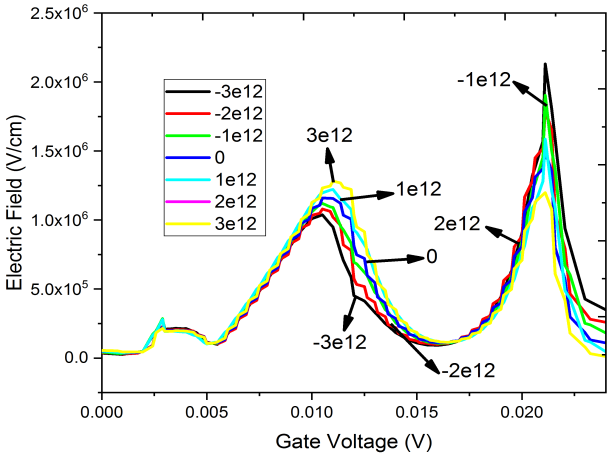


Fig. 11: Net Electric field distribution of SSSC-FinFET

The electron concentration distribution of SSSC-FinFET and ASSC-FinFET shown in Figure 7 and Figure 8 respectively exhibit similar trends as the gate voltage increases. In both cases, the electron concentration decreases initially, reaches a minimum, and then rises again. However, the magnitude and sensitivity of these changes differ between the two designs. For the symmetrical source, the electron concentration varies significantly with different interface charges, as indicated by the noticeable separation between the curves. This suggests that the electron concentration in the symmetrical source design is highly sensitive to interface charges, which can introduce instability in device performance under different operating conditions. The broader range of electron concentration in this design can lead to higher

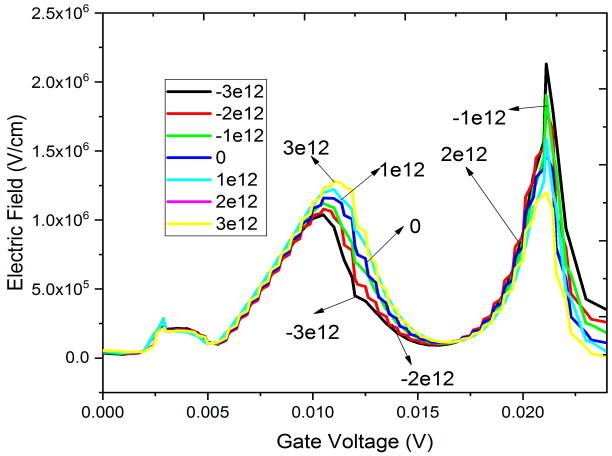


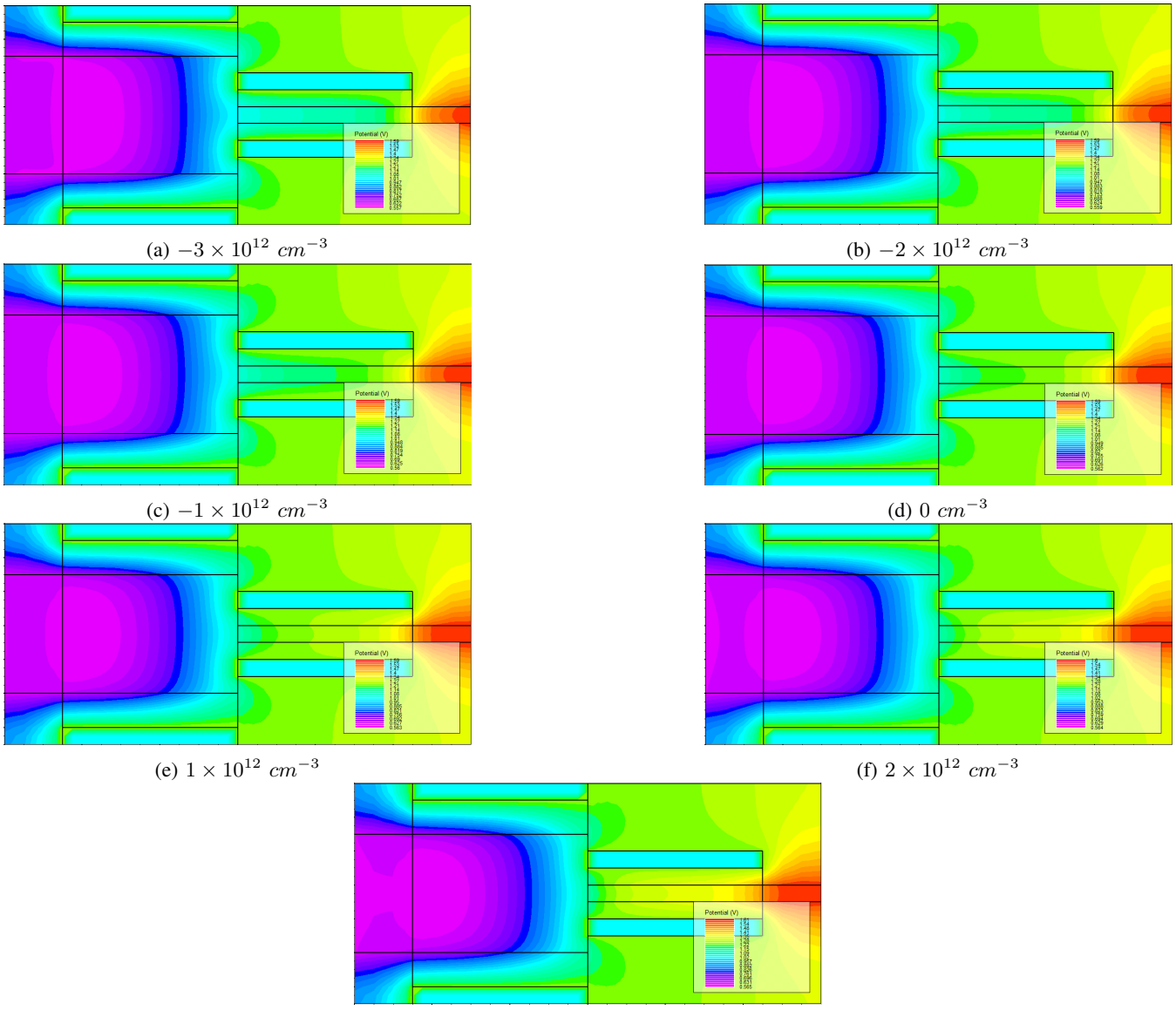
Fig. 12: Net Electric field distribution of ASSC-FinFET

variability in electrical characteristics, potentially impacting the reliability of the device. In contrast, the asymmetrical source design shows less pronounced variation in electron concentration across different interface charges. The curves are more closely grouped, indicating a reduced sensitivity to interface charges. This stabilization of electron concentration in the asymmetrical source design results in more consistent device behavior, enhancing performance predictability. The control over electron concentration as a function of gate voltage is also better in the asymmetrical source design, suggesting improved control over channel formation and carrier distribution.

Figure 9 and Figure 10 shows Lateral electric field distribution of SSSC-FinFET and ASSC-FinFET. In both Figures, there is a noticeable peak in the lateral electric field as the gate voltage increases. However, the magnitude and behavior of this peak differ between the two configurations. In case of SSSC-FinFET the peaks are relatively higher, with more pronounced variation in the electric field as the interface charge changes. Table 2 compares the drain current characteristics.

The electric field is more symmetrical across different interface charges, showing uniformity but potentially higher values in unwanted regions. The effect of interface charges appears to be more pronounced, leading to higher fluctuations in the electric field. This suggests a stronger dependence on interface charges, which could be detrimental under varying operating conditions. In case of ASSC-FinFET the peaks are generally lower, indicating a reduced maximum lateral electric field, which is more desirable for minimizing short-channel effects and improving device reliability. The asymmetry in the source design results in a more tailored electric field distribution, reducing the electric field in critical areas, thereby improving device performance by lowering leakage currents and reducing hot-carrier effects. The fluctuations due to interface charges are more controlled, indicating that the asymmetrical source design helps stabilize the electric field across varying charges, enhancing device robustness.

The asymmetrical source design, as shown in the Figure 6, provides a smoother lateral electric field distribution, which is crucial for reducing short-channel effects, improving subthreshold slope, and enhancing overall device performance. The reduction in peak electric field values is particularly im-



(a) $-3 \times 10^{12}\ cm^{-3}$ (b) $-2 \times 10^{12}\ cm^{-3}$

(c) $-1 \times 10^{12}\ cm^{-3}$ (d) $0\ cm^{-3}$

(e) $1 \times 10^{12}\ cm^{-3}$ (f) $2 \times 10^{12}\ cm^{-3}$

(g) $3 \times 10^{12}\ cm^{-3}$

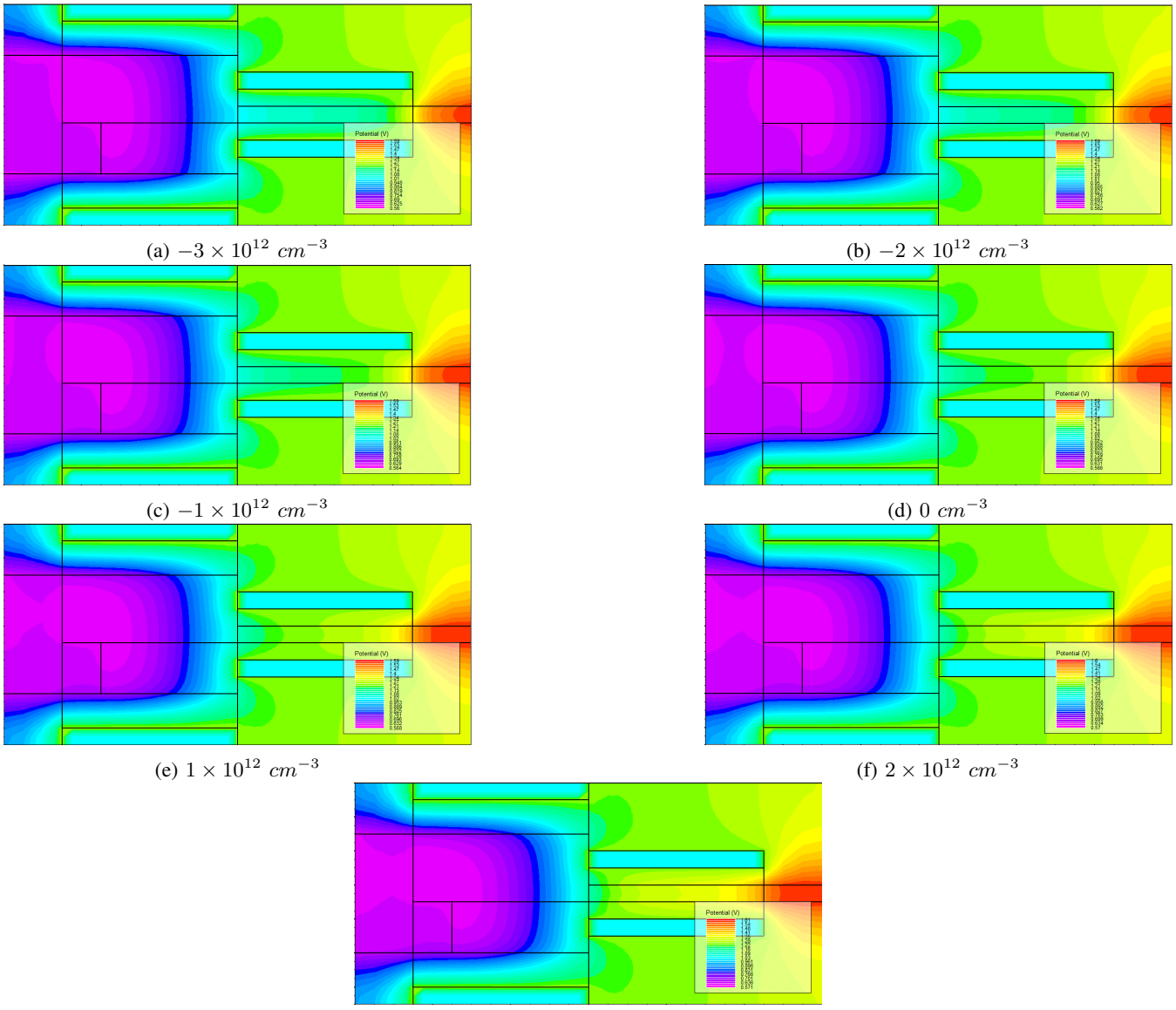
Fig. 13: Contours of Potential distribution for different interface charge concentrations of SSSC-FinFET

portant for increasing the device's longevity and reliability by minimizing degradation mechanisms. Asymmetrical source design leads to a significant reduction in peak lateral electric fields, which helps mitigate hot-carrier injection and other high-field-related reliability issues.

The Net electric field distribution of SSSC-FinFET and ASSC-FinFET is shown in Figure 11 and Figure 12. In case of SSSC-FinFET, the electric field distribution shows a clear pattern of peaks and valleys as the gate voltage increases. These peaks likely correspond to regions where the electric field is highly concentrated, possibly at the edges of the gate or at junctions between different material regions within the device. The effect of the interface charge is evident as the curves shift slightly depending on the magnitude of the charge. For negative interface charges, the electric field peaks tend to be lower, indicating that the charge may be partially counteracting the electric field induced by the gate. Conversely, positive interface charges increase the field strength, leading to higher peaks.

In case of ASSC-FinFET, similar pattern in the electric field distribution but with some key differences. The asymmetry in the source appears to affect the electric field distribution, particularly in how the peaks align with respect to the gate voltage. The peaks in this graph are slightly more pronounced for both negative and positive interface charges, suggesting that the asymmetrical source introduces additional factors that intensify the electric field at certain points. This could be due to the uneven distribution of the electric potential across the device, caused by the asymmetry in the source.

When comparing net electric field of SSSC-FinFET and ASSC-FinFET, it is evident that the asymmetrical source alters the electric field distribution, making the device more sensitive to changes in interface charge. This could lead to enhanced control over the device's switching behavior, as the gate voltage has a more pronounced effect on the electric field in the asymmetrical source configuration. However, it may also introduce challenges, such as increased electric field intensity at certain points, which could lead to higher leakage currents or even breakdown under extreme conditions. Table



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(g) $3 \times 10^{12}\ cm^{-3}$

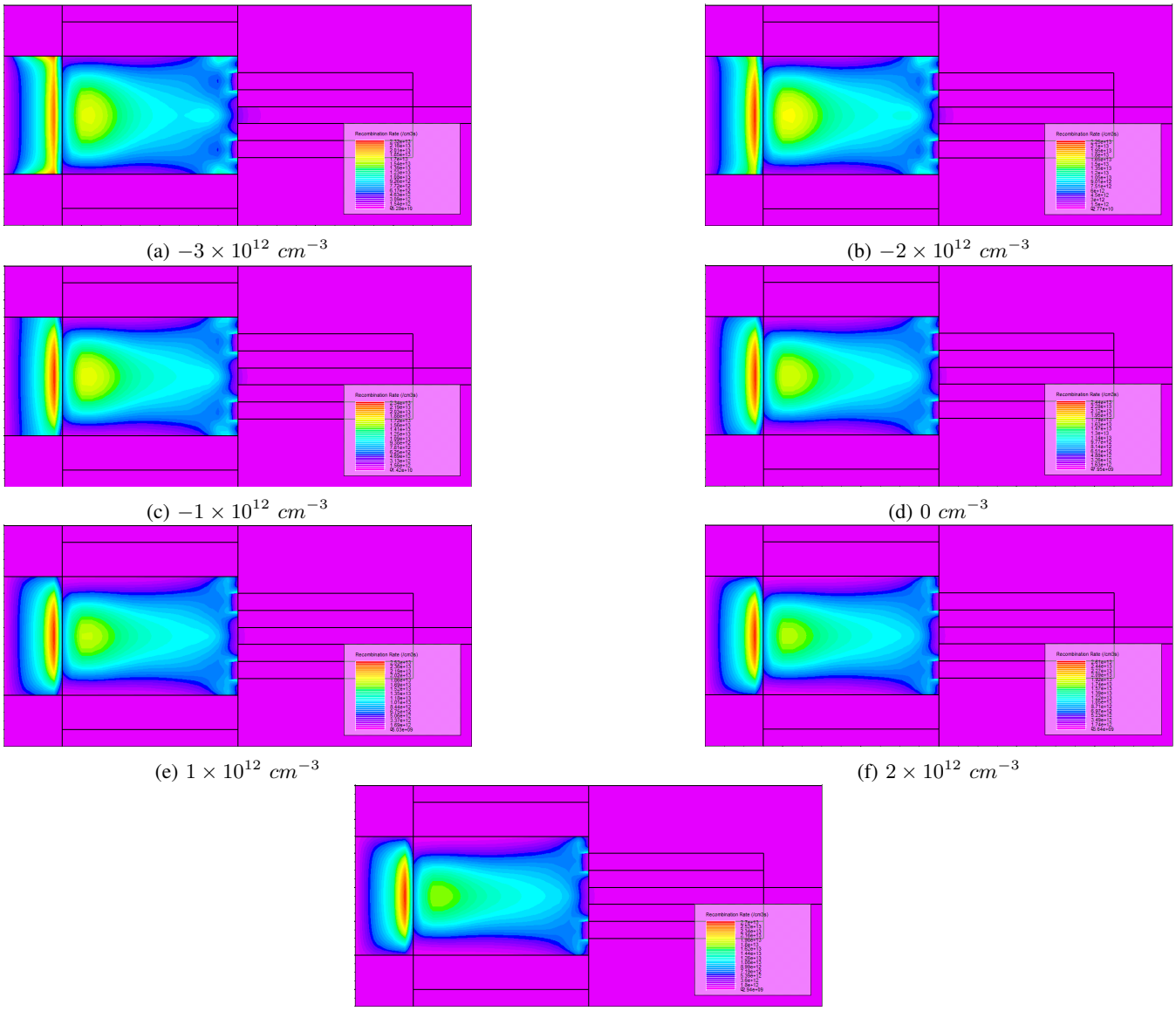
Fig. 14: Contours of Potential distribution for different interface charge concentrations of ASSC-FinFET

3 compares the electrical performance parameters.

Figure 13, which depicts the contours of the SSSC-FinFET, is seen to be influenced strongly by the charge concentrations at the interface. The patterns are highly irregular and fairly well spaced apart. For higher negative charge concentrations, the drop in potential near the source is sharp with a steep gradient of electric field. For positive charge concentration, the increase in potential is prominently visible. Such behavior typifies the sensitivity of the device towards interface charges that tend to distort uniformity in the electric field and result in relatively unstable formation of the channel. A spiky variation of spacing along contour points suggests irregularities in electric field arrangements within the channel, which may adversely affect the coherence of carrier transport and device performance.

Figure 14 shows the Contours of potential for the ASSC-FinFET are more or less very stable and uniform with different interface charge concentrations. This asymmetrical source design greatly affects suppressing such influences from interfacial charges by redistributing electric field in the channel. With negative interface charge concentrations, the potential drop near the source is much gentler to avoid abrupt transitions altogether and maintains better stability in the channel. Indeed, in the positive charge concentration regimes, potential boosting is better controlled in order not to generate the strong peaks as shown in the SSSC-FinFET. The closely spaced and relatively uniform contours in the ASSC-FinFET indicate improved electrostatic control and reduced sensitivity of the device to interface charges, hence more predictable behavior of the device.

Due to the increase in the effects of such interface charge concentrations and the resulting interface traps, causing abrupt potential distribution, this will lead to uneven carrier distribution and a higher electrical field variability and may eventually degrade reliability. Conversely, in ASSC-FinFET since it supports extended geometry of the source, this one contains better electric field modulation also elevating its resistance against the influence of the different charges at the interfaces. This design provides smoother potential distribution, which facilitates better formation of channels



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(g) $3 \times 10^{12}\ cm^{-3}$

Fig. 15: Contours of Recombination rate for different interface charge concentrations of SSSC-FinFET

TABLE II: Comparison of Drain current performance parameters

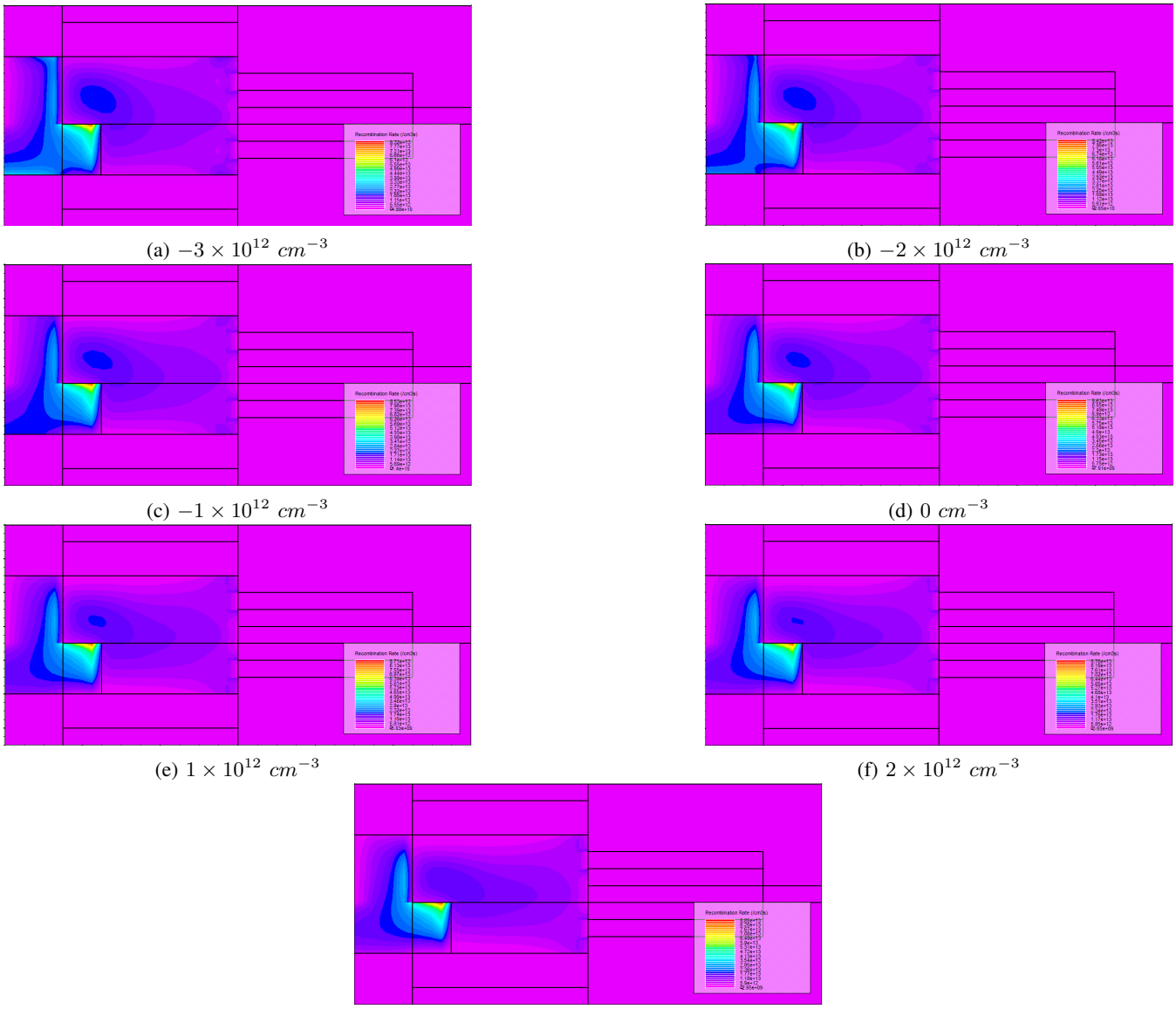
Type of Device	Interface charge in cm-3	Ioff (A)	Ion (A)	Ion/Ioff	Vt (V)
SSSC FinFET	-3e12	9.6e-12	0.12m	1.2e7	0.271
	-2e12	5.7e-11	0.14m	2.5e6	0.214
	-1e12	3.4e-10	0.17m	501556	0.172
	0	2.3e-9	0.2m	302484	0.082
	1e12	1.2e-8	0.25m	21140	0.059
	2e12	3.9e-8	0.3m	7758	0.0266
	3e12	1.12e-7	0.36	3238	-
ASSC FinFET	-3e12	9.7e-12	0.13m	1.38e7	0.26
	-2e12	5.78e-11	0.16m	2.79e6	0.21
	-1e12	3.49e-10	0.19m	552046	0.17
	0	2.05e-9	0.23m	112760	0.11
	1e12	1.21e-8	0.27m	22905	0.056
	2e12	4.9e-8	0.33m	6839	0.02
	3e12	1.4e-7	0.40m	2841	-

TABLE III: Comparison of Electrical performance parameters

Type of Device	Interface charge in cm-3	Emax (MV/cm)	Emin (mV/cm)	Ex,max (mV/cm)	Ex,min (MV/cm)
SSSC FinFET	-3e12	2.17	1.19	356	-2.17
	-2e12	1.78	0.96	370	-1.78
	-1e12	1.85	3.08	333	-1.85
	0	1.48	5.23	273	-1.48
	1e12	1.57	7.43	334	-1.57
	2e12	1.2	6.12	349	-1.2
	3e12	1.26	1.74	261	-1.26
ASSC FinFET	-3e12	2.13	26.5	257	-2.13
	-2e12	1.79	29.3	211	-1.79
	-1e12	1.9	32.2	266	-1.9
	0	1.49	36.4	204	-1.49
	1e12	1.59	39.5	258	-1.59
	2e12	1.28	12.5	197	-0.5
	3e12	1.34	43.9	251	-1.34

and reduces the chances of performance failures. The ASSC FinFET will be considered a more reliable solution for high-performance applications because it controls the stabilization of potential contours under different conditions.

In Figure 15 recombination rate contours for the SSSC-FinFET show a high variability depending on the concentra-



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(g) $3 \times 10^{12}\ cm^{-3}$

Fig. 16: Contours of Recombination rate for different interface charge concentrations of ASSC-FinFET

tion of charge in the interface. For higher negative charge concentrations ($-3 \times 10^{12}\ cm^{-3}$), the recombination rate is smaller close to source and drain regions, increasing abruptly in localized areas inside the channel. This indicates that the symmetrical source architecture is failing in distributing the electric field uniformly leading to hotspots of strong recombination. The recombination rate also increases disproportionately near the source-channel and drain-channel interfaces at positive charge concentrations ($3 \times 10^{12}\ cm^{-3}$). These sharp gradients in recombination are indicative of the high sensitivity of the device to interface charges, which disrupt carrier flow and lead to non-uniform channel behavior. The irregular spacing of contours further emphasizes the inconsistency in recombination rates through the channel, and thus impacts device reliability and efficiency.

The recombination rate contours of the ASSC-FinFET in Figure 16 are much smoother and uniform for all the concentrations of interface charge. In nature, source design now becomes asymmetrical, and this itself proves to be very effective in reducing the influence of interface charges by allowing better control over electric field and charge distribution. At negative interface charges, recombination rate is fairly low throughout the channel, thereby preventing the localized spikes seen in the SSSC-FinFET. With positive interface charges, there is a slight increase in recombination, but it is homogeneously spread, thereby eliminating sharp changes. Uniformity is the hallmark in this regard as the ASSC-FinFET shows strength in sustaining steady-state carrier dynamics even while fluctuating in interfacial charge concentration. Close spacings indicate an improvement in electrostatic control with a predictable recombination profile in support of reliable device operation.

The comparison of the two designs highlights the superior recombination rate management capabilities in the ASSC-FinFET. In SSSC-FinFET, the source asymmetry enhances the influence of fluctuations in interface charge, which implies irregular recombination and unbalanced transport of carriers. This may yield higher dissipated power and reduced performance. The asymmetrical source geometry in the ASSC-FinFET optimizes the carrier flow and elec-

tric field distribution for consistent recombination behavior. Hence, the contours in figure 16 are more smooth and predictable as ASSC FinFET has acquired its ability to minimize the recombination losses, thus becoming a more reliable choice for applications of high-performance energy-efficient transistors.

In conclusion, the step-channel FinFET with an asymmetrical source shows a modified electric field distribution compared to the standard step-channel FinFET. The asymmetry in the source appears to enhance the sensitivity of the device to interface charges, potentially offering better control but also introducing risks associated with higher electric field intensities. These findings suggest that while asymmetrical source designs may provide benefits in certain applications, careful consideration must be given to the potential trade-offs in device reliability and performance.

IV. Conclusion

The study demonstrates the superior performance of the Asymmetrical Source Step Channel Double Gate FinFET (ASSC-FinFET) compared to its symmetrical counterpart. The ASSC-FinFET shows better control over electron concentration and lateral electric fields, which significantly reduces the short-channel effects and enhances device reliability. The findings reveal that the asymmetry in the source leads to a smoother lateral electric field distribution, minimizing the risk of hot-carrier effects and leakage currents. Moreover, the ASSC-FinFET's reduced sensitivity to interface charges further contributes to its stability and performance predictability. While the asymmetrical design introduces complexities in electric field management, its advantages in scalability and energy efficiency make it a strong candidate for future high-performance semiconductor applications. Continued research in optimizing the fabrication processes and understanding the trade-offs in device reliability will be crucial in realizing the full potential of ASSC-FinFETs in commercial applications.

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