An Intelligent Network Router based on Data Segregation

Sumana Achar, Jayadevappa D.

Abstract—**Large data packets that exceed the networks' transmission capacity cause congestion and lead to excessive network bandwidth usage. A crucial component of data segregation based on data characteristics has been overlooked by majority of the existing commercial routers that are dependent on software algorithms. To comprehend network topology and boost routing performance, deep learning techniques are now in use to make routing decisions. Most of the time data's size, rate and duration are not measured by the data transmitter or receiver. This study proposes designs for Intelligent Routers. Usually, data analysis and processing procedures were done at the transmission end and was not a component of the router. However, we have configured the router to decide whether to separate the data before routing in accordance with user preferences and available channel capacity. This innovative architecture divides data according to size, length, and rate for a dense network, enabling the router to act intelligently while sending data across the channel. Massive data accumulation and resource consumption will decrease in real time on the part of service providers. To lessen the strain on devices and data monitoring at the exchange, we assert that this Intelligent Router can be positioned anywhere in the network hierarchy depending on utilization, either in edge routers or at the exchange. The proposed Intelligent Router consumes 60–65 mW power, which is 85.7-89.9% less than software algorithm-based routing methods. When compared to a few software routing strategies cited in this paper, the critical path latency for data transmission in proposed Intelligent Router is 10.915 ns, which results in a 9-fold increase in data transfer speed.**

Index Terms — **Network congestion, data segregation, intelligent router, traffic management.**

I. Introduction

ROUTER design is a challenging task in the urban areas due to random delay and unspecified congestion. Data transmission delay is the major metric for packet transfer[1]. Machine learning is used to optimize routing, adjusting delivery routes in real time[2]. Using an online-algorithm method, data may be gathered over 5-10 minutes time in a network to produce steady routing performance. Online algorithm cannot be applied to short time data whose longevity is less than 5 minutes [23]. Data clogging usually happens at local exchanges due to long duration data requests blocking short duration data requests. In such cases router must be capable of segregating data based on time-duration and then allow data transmission to ease network congestion. This leads to effective and optimized use of channel bandwidth. Data segregation will significantly reduce redundant-requests buffering at the routers. Because routers can make judgments based on data attributes, they will function as network processors, lightening the strain on the data-influx management system.

Dynamic situation of data connectivity exists as users and exchange will have any recommendations beforehand, on the data span and the data connectedness time will extend based on the size of files used to download/upload on to a server and during live streaming of video/audio files. Whenever the network size increases, the protocol prolongs the data delivery [3]. By segregating the data based on its features, data format will not change and can be effortlessly arbitrated. Arbitration procedure [4] is used to separate data and traffic before making the proper routing decisions. Data rate can change depending on whether network is dial-up /2G /3G /4G /broadband /fiber-net according to protocol used for internet service. Data services, such as social media and the internet, function at inflated data rates or higher speeds than voice communications, which often have transmission and reception dilatory.

Utilizing a single antenna, voice and data modulated signals are sent and received. As examined in the majority of modern telecom routing situations as 4G and above generations, we get to see same router operating at variable routing rates. But in 2G and 3G communication for voice and data, routing is done using separate bandwidth and channels. In 4G and beyond 4G, voice will be remodeled into data and voice combined data will be sent over channels. Hence data operators provide internet with unlimited talk-time and limited data at affordable cost. Since a high-speed data channel bandwidth is roughly equal to a big ratio of data channel bandwidths, only data is charged. At the exchange level, bandwidth is high compared to 2G/3G. So overhead, data rate and infra utilization reduces.

The implications on speed, bandwidth-usage and tariff is that each user needs a dedicated high speed router and channel for data upload/download. As a result, creating a plan to separate high- and low-data-rate signals at the provincial exchange or routing level is imperative. Sometimes the data magnitude will be known to the downloader before the request-to-download because file size is updated in the internet browser. Browser will also indicate the percentage of file size being downloaded.

Manuscript received October 3, 2023; revised October 30, 2024.

Sumana Achar is a Research Scholar at Department of Electronics and Instrumentation Engineering, JSS Academy of Technical Education Bengaluru, affiliated to VTU Belagavi, India. (Corresponding author: Phone: 8971605150; e-mail: sumanavtuphd@gmail.com)

Jayadevappa D. is the Principal of Dr. H.N. National College of Engineering, Bengaluru, affiliated to VTU Belagavi, India, (Phone: 9986134424; e-mail: devappa.22@gmail.com)

Hence this information can be useful if the router segregates the data based on its magnitude. Hence there is an essential requirement to devise a smart routing mechanism to solve aforestated arduous technical complications, which has serious performance repercussions.

Many research is carried on software routing algorithm and its optimization. Most of the routers that exist today are hybrid routers that depend on operating system to handle and control the data routing. All the routers that are in market are ASIC based and their scope for design reuse is not possible. FPGA based design will give scope for design re-use. By dividing data according to rate, duration, and size, routers may route data more efficiently, resulting in less traffic jams and less resource use. In this paper, a unique digital design of routing technique with data segregation is proposed which make it an intelligent network router. The design's performance feature comparison and simulation results are examined.

II. Literature Survey

Wireless network needs optimal route for data forwarding. The delay matrix calculated for the network topology must suggest the optimized route with minimum delay[1]. Efficiency of data transmission can be more improved if data is segregated before routing to reduce overhead of the network. Data aggregation should be considered to prevent redundant-duplicate data being sent to Base station [5].This establishes the audit trail on Data [6]. It is necessary to conduct evaluation with more training data in order to evaluate the effectiveness of routing decisions. We investigate that many routing algorithms like Group based algorithm [7], adaptive routing, Q-adaptive routing, Fuzzy Logic approach exist which can be applied for various network topology, but they prove their efficiency on CPU based software routers [8, 9]. Ant colony optimization methods, meta heuristic algorithms and its combinations are also implemented on software routers for achieving best optimization in algorithm processing time[10, 11].

An Intelligent-on-chip transport system can be achieved with an efficient routing protocol [12] and resource management [13]. Characteristics of the data and availability of its storage in different domain will quantify the benefits in bandwidth utilization during traffic congestion [14].

Varying data rates will largely imapct the performance of the system in multipath routing [15] , Majority of the existing network routers are software algorithm-based routers and data rate, packet loss, throughput, latency, memory utilization is measured using software. Limitations of CPU will not give high speed data transmission, instead it lays a path for embedded FPGA based Network Router[16].

Multiple propagation paths exists in network to transmit the data from one base station to the destination base station and if more delay in data transmission seen, the maximum data rate range is also minimum [17]. The current 5G and 6G network in the future with ultra-high density, bandwidth, mobility, and large scale requires highly efficient end-to-end optimization methods. Deep Learning methods attracts the research area in such network optimization and makes the network Router Intelligent[18].

A very few research works are found on FPGA routers based on data characterization and using their property to intelligently transmit the data on network. An observation says, that the software routers are playing a major role and hence most algorithm dependent research has been taken place and has achieved significant performance. Data acquisition irrespective of their rate and size is done in existing routers and the data is routed on the network on a single channel where power consumption for a small sized data seems to be huge.

III. Proposed Methodology

The router top-level module shown in Fig. 1 is the main research work that aim towards efficient design of multi-functional FPGA router architecture. Basic protocols used by the routers acts as preliminary base work for the current proposed architecture [19]. In this paper, Intelligent/Smart router architecture is proposed as shown in Fig.2, which is a sub-module of the top-level architecture shown in Fig. 1.

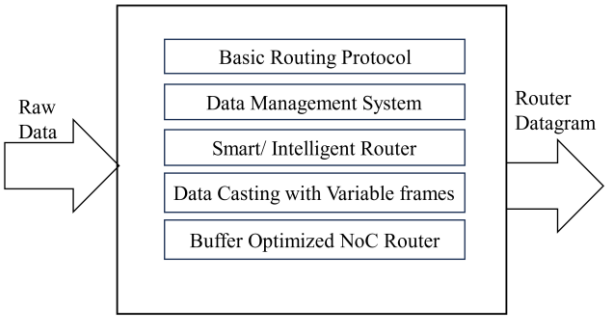


Fig. 1. Top-Level Router Architecture

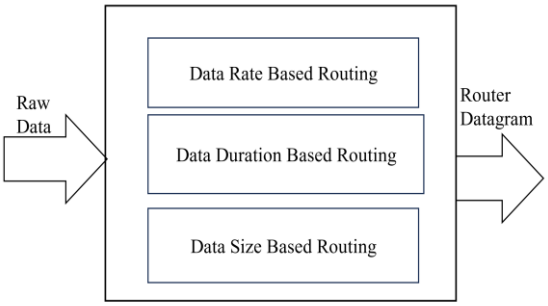


Fig. 2. Proposed Intelligent/ Smart Router Architecture

Smart or Intelligent Routing can be classified into three types:

i. Routing based on Data Rate
ii. Routing based on time (Data Duration)
iii. Intelligent Routing based on Data Size

A. Data Rate based Intelligent Routing (DRIR)

Need for DRIR

Amount of data transmitted per specific period is data rate. It determines the speed at which the data is transmitted between the two routers as well as between a router and the peripheral end user. If the data rate is less compared to the bandwidth, then data transmissions take place at lower speed, though channel has the capacity to transfer at high speed. Similarly, limited channel capacity less than the data

rate can lead to packet loss. This effects the performance of the system. Network may get terminated due to this imbalance to sense the data packets. Hence there is a strong need to segregate data on a common line as Low and High-speed data. It is also noted that data transfer rate differs based on media. Data-rate is measured in either bits-per-second(bps) or bytes-per-second (Bps). Data-rate is the benchmark to assess the performance of the communication channel and many developments are made to increase the data rate for 5G communication. Noise characterization will be affected as bandwidth will be limited. Data-rate varies from user-to-user and device-to-device. Practically in real-time, data segregation is complicated task. Segregating data as Low Data Rate (LDR) and High Data Rate (HDR) and mixing them before transmission and channeling into a single common data line is needed. Two approaches of segregation can be proposed depending on analog signal and another based on digital data, like Method of encryption and Pulse-Count method repectively.

Method of Encryption

Three stages listed below are used to seperate rate of data which are featured as analog,

i. Use any precise frequency to volatge converter.
ii. Transform voltage into digital bits by means of an advanced resolution Analog to Digital Converter (ADC).
iii. The four MSB bits from ADC output can indicate High Data Rate (HDR) or Low Data Rate (LDR) as depicted in Table I.

TABLE I
ENCRYPTION TO SEGREGATE FREQUENCY OF DATA

Frequency in Hz	Voltage(V)	8-bit digital encryption Bits
LDR 1KHz	1	0000XXXX
HDR 1 MHz	5	1111XXXX

There are few drawbacks in encryption method. It is difficult to acheive efficiency and resulution in the output of F to V converters' and ADC. Also, large hardware overhead exists. This 3-level complex process is a static read back process (not live Data Rate separation). Hence to acheive accuracy an alternate method has to be chosen or the design has to optimised for better efficiency and resolution of output.

Pulse Count Method to separate Data Rate

In 4G communication and above, On a shared data line, audio and data must be received separately and processed separately. Voice data needs to be played back in speaker mode, while data needs to be processed, shown, or played in the format that it belongs to. The pulse count method counts the number of pulses that arrive at the router in a second and chooses the best segregation technique to put LDR on one channel and HDR on another channel. In practice, router may receive either LDR only or HDR only or both HDR and LDR or nothing (i.e., neither HDR nor LDR). Sensing No-Data-Rate situation and designing a system for such no no-signal that randomly arise is a challenge due to uncertainty. We should indicate no-data-occurance through transmission channel. In this HDR and LDR separation, a threshold count pulses/secs will be kept as reference threshold to demarcate low Data Rate and high data rate. The amount of traffic on the network determines this threshold count. An incoming data set is classified as High Data Rate if the count value exceeds the threshold, and Low Data Rate otherwise. Data rate usually decreases by reducing allocated bit duration. But reducing bit duration is helpful for receivers with good sensitivity.

Digital Design of DRIR

The Fig.3 is the digital design of Data Rate based Intelligent Router. The comparator in the design has three outputs: PR<RR; PR=RR; PR>RR based on Data duration. In this, voice data (voice converted into digital data) and broadband data will be coming into common data line of Router. The Router must apply its intelligence and segregate HDR and LDR. This is achieved by a method where, Unified data (broadband data + voice) is applied to the pulse counter which will count the number of pulses. The pulse counter's output is linked to a pulse register, which counts the number of pulses. The size of reference register is equal to size of pulse register. The comparator, which may separate data based on data rates, is coupled to the output of the reference register and pulse register. High frequency clock is divided using accurate time base generator until one-second pulse is generated.

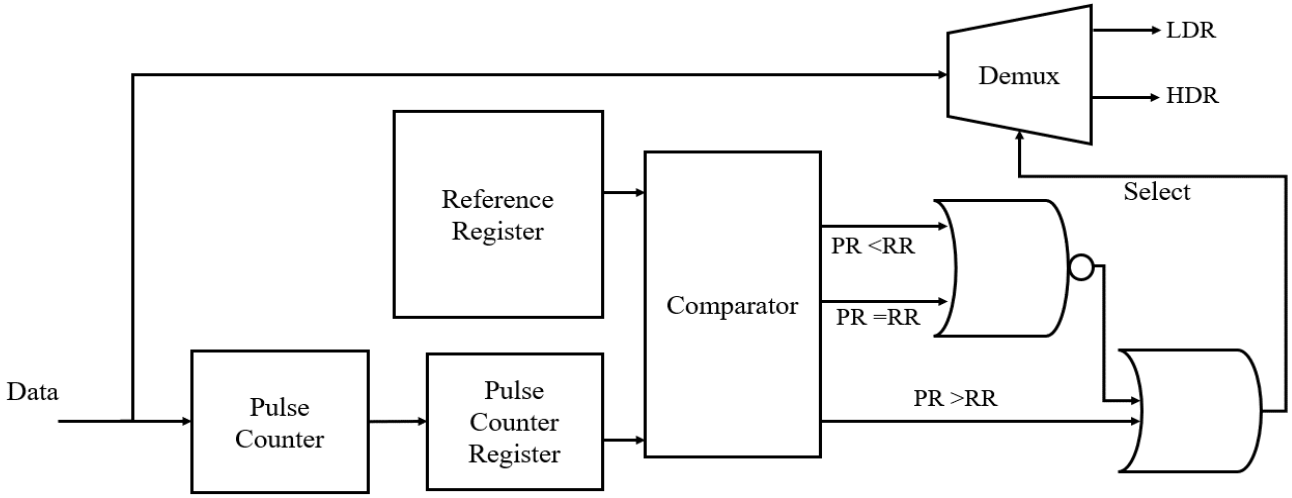
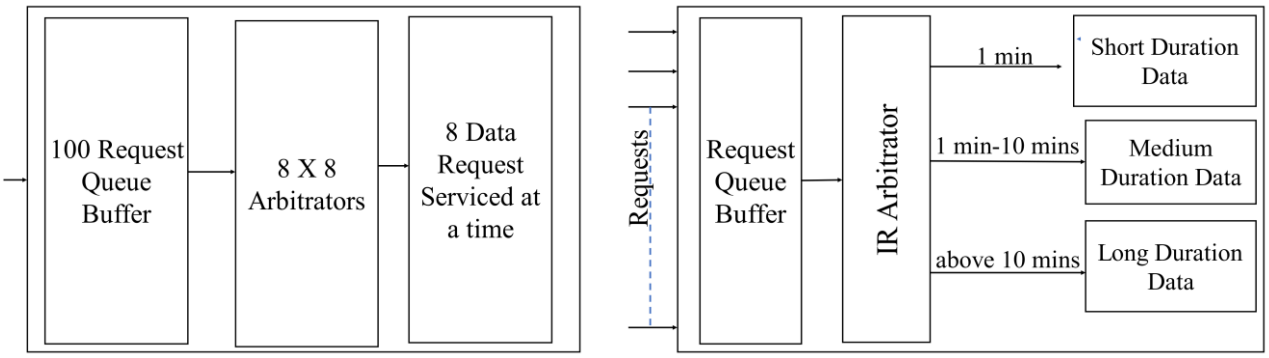


Fig. 3 Digital design of Data Rate based Intelligent Router



(a) (b)

Fig. 4 (a) Buffered ROUTER [8x8] with Router taking 8 service requests at a time leading to pile up (b) Request queue buffer with short, medium, long data segregation

B. Data Duration based Intelligent Router (DDIR)

Need for DDIR

Network's end users and users of certain service providers amongst inter/intra circle may not know the duration of data they use, priorly. The data duration may be less than a minute and some data may stay for long hours.

In the event of peak hour data traffic, massive backlog of data requests will occur, if the data is maintained on the line for an extended period. Only eight requests (on priority) are taken at a time from a 100-request queue in the request buffer depicted in Fig. 4(a). Till these initial eight batches of requests are fulfilled, all other requests will need to wait. Thus, only eight requests are capable of being processed by this network router at once. This results in massive backlog of inquiries, which causes extreme queue buffer congestion.

Resource contention can be brought down systematically. This problem can be solved by using the Intelligent Routing by using three level time duration arbitration as seen in Fig. 4(b). Data requests are arbitrated based on duration of data and en-routed to the respective channels. Studies suggest that 70% data durations are less than a minute. Therefore, by utilizing a structure similar to the one depicted in Fig. 4(b) and a 7:2:1 ratio of short, medium, and long data routers, we can effectively handle the hundred-request queue build up and service it successfully.

A high competition exists among telecom operators, who offer unlimited free and low-cost call rates to its subscribers. It becomes essential to divide and route data and calls with varying durations. Routing resources are wasted at the service suppliers' end and automatic data routing at continuous connectivity is impossible without intelligent routing. So, the routing infrastructure must be designed in chosing one criteria from stated below:

i. Single Router must process the data seperation data on its duration.
ii. Deploy suitable number of routers in the ratio of data duration.

Digital Design of DRIR

The intricacy of segregating data based on data duration is difficult, since neither the sender nor the recipient will be aware of the previous information on the data-duration. This adds lot of uncertainity and obscurity in routing and router system design.

Digital data is made to hit data routing blocks (scalable) such as Short Duration Data Routing (SDDR) logic, Medium Duration Data Routing (MDDR) logic and Long Duration Data Router (LDDR) logic. In our experimental test case, we have quantified and stratified the data presence in Table II.

TABLE II
CLASSIFICATION OF DATA DURATION BASED ON DATA PULSES

Data Duration	Data Pulses	Data Routing
Short duration Data	0 to 5	SDDR
Medium duration Data	6 to 9	MDDR
Long Duration Data	Above 10 Pulses	LDDR

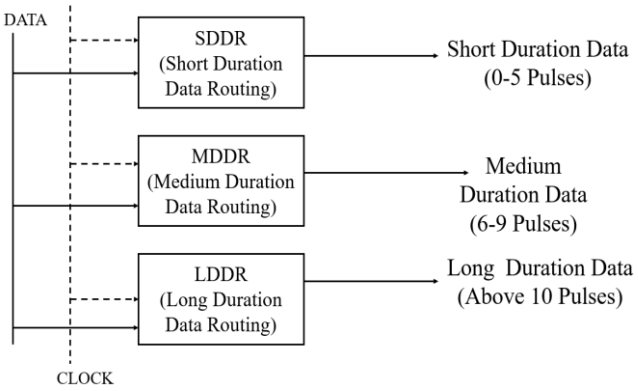


Fig. 5. Block Diagram of Data Duration-based Intelligent Router (DDIR)

Block diagram of Data Duration-based Intelligent Router is shown in Fig. 5. Here,

i. SDDR will have counter that counts pulses from the data line. If the data persists up to few seconds less than a minute (set as threshold level for data duration and can be varied by network administrator at exchange level), then the data is classified as short duration data and hence routed accordingly over the channel recognised for short-duration.
ii. If data persist for duration ranging between 1-10 mins, then, it is classified as medium duration data.
iii. And if data duration is above 10 mins, then it is classified as long duration data.

The design requires dedicated resources and separate

channels for segregated data. The digital design for Data Duration based Intelligent Router is shown in Fig. 6. Data segregator is designed based on data rates as shown in Table II. Here, Data and clock signals are applied to Mod 5 counter. If Data signal persists up to first 4 clock cycles, then this data will be segregated as Short Duration Data (SDD). If the same data persist for more than 5 clock cycles, data gets classified as Medium Duration Data (MDD).

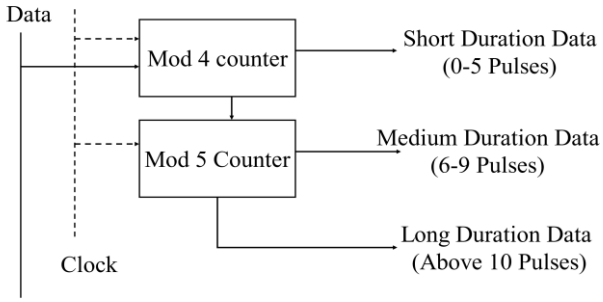


Fig. 6 Digital Design for Data Duration based Intelligent Router (DDIR)

In the design, the terminal count (TC) of Mod 5 counter is tracked for first both SDD and MDD types of data segregations. The Mod 5 counter output is fed to another Mod 4 counter. This mod 4 counter counts to 9 clock cycles of data presence. If the data persists for 5 to 9 clock cycles, the data is treated as medium duration data and hence routed to MDDR channel. If data persists beyond 9 clock cycles, the terminal count of Mod 4 counter goes high and the data present beyond this threshold of 9 clock pulses shall classify the corresponding data as Long Data Duration. Hence this data will be routed to Long Data Duration Router (LDDR) channel. MDDR is tri-stated as data is routed through LDDR. Data is routed through LDDR primarily until the reset command is applied once more. System is reset to process new set of data after limited set of packets.

C. Data Size based Intelligent Router (DSIR)

Need for DSIR

In any file transfers, there exists small sized data and bulk data. For instance, consumers may download files, few may utilize data links merely for surfing, while rest may spend several hours watching live sports. Therefore, it is imperative to distinguish between users of low volume data and those using bulk or huge data. Thereby these low-volume-data users can be mapped onto Normal Data Path and bulk-data users can be mapped onto Bulk Data Path.

As illustrated in Fig. 7, this routing strategy is comparable to Direct Memory Access (DMA), which allocates a channel for bulk data transmission between IOs and memory in a processor environment.

For transfer of data from memory to I/O or vice versa, Direct Memory Access (DMA) type of protocol is used to transfer bulk data in a dedicated data path after the handshake is done to check busy and idle states of data transmitter and receiver. In the next step, the DMA protocol will check whether the data size qualifies for allocation of data path for bulk data transfer. The access time is reduced by using DMA controller.

Routing can be done without any interference of CPU (Computer Processing Unit) which usually adds latency to the routing process. Aim is to make the router to act like a network processor independent of main CPU. Similarly, the arbitration logic and the data segregation unit in the Intelligent Router can reduce the use of CPU and hence the critical path delay can be highly improved for the proposed router.

A lot of data processing units work on fixed length data. Suppose we have the data of larger bytes and protocol has the fixed-size frame whose size is lesser than the size of data to be transmitted, then the frame is padded with zeros. Hence there is a trade-off when variable length data sits on a fixed size frame length. This padding generally uses more design resources.

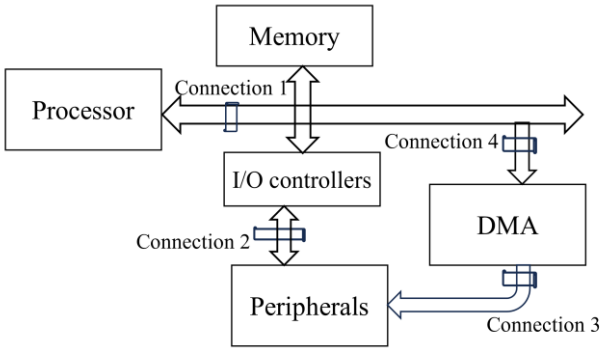


Fig. 7 DMA for Bulk Data Transfer

In normal software protocols and asynchronous communication, a data frame's header and footer will provide information about the amount of data in bits or bytes. This will help certain type of data arbitrators to separate normal data from bulk data. The channels can be classified as byte, kilo-bytes, and mega-bytes channel when size-based routing is implemented. Edge-users can use data line for email checking, advanced search/ browsing, downloading data files, images, and live video streaming.

Digital Design of DSIR

Block diagram of DSIR is shown in Fig. 8 and its respective digital design is shown in Fig. 9.

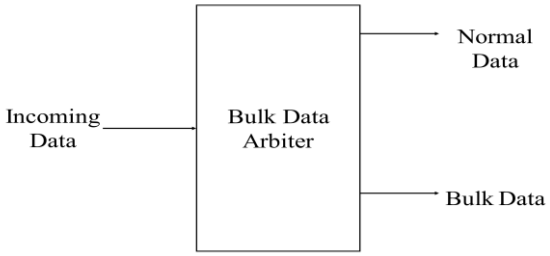


Fig. 8 Block diagram of Data Size-based Intelligent Router (DSIR)

In the digital design of DSIR shown in Fig. 9 Regular data and bulk data are distinguished using a byte counter and a demultiplexer. In this instance, input data is applied to the Demultiplexer and supplied to the byte counter's count input as well. Aligned with the clock input, the byte counter keeps track of the bits/bytes present in the data. Assuming that the byte counter is intended to count 100

bits per second, the terminal count (TC) signal will change to 1 as soon as the byte counter hits 100 bits. The signal is attached to the demultiplexer's select line when TC=1. The byte counter count value (TC=0) indicates that the input data is translated to the normal/ regular path (out1 of the demultiplexer) until it is less than 100. When the byte count value hits 100, the input data is translated down to bulk data, TC becomes 1, and the demultiplexer's select line also becomes 1.

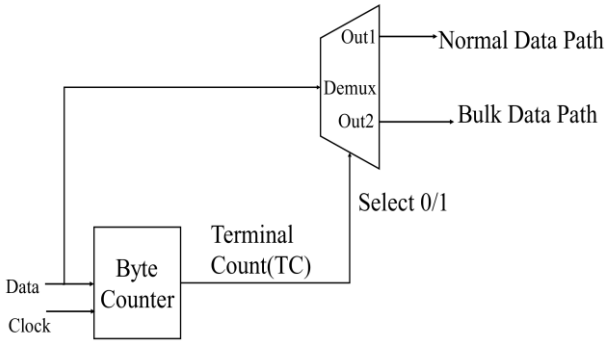


Fig. 9 Digital design of Data Size-based Intelligent Router (DSIR)

When routing between normal and bulk data, a First-in-First-out (FIFO) buffer can be utilized to store input data to prevent data loss by missing of any data during transmission. Every aspect of the architecture is entirely programmable and scalable. User programming allows for control over the number of bulk data levels and bulk data size definitions.

To prevent retransmission and data loss during each transfer of input data from the normal channel to the bulk channel, appropriate line buffers can be employed to gather and aggregate both normal and bulk data.

IV. Results and Discussion

Digital design for the proposed work is accomplished to meet required router functionality. Verilog code is written for the proposed digital design in the HDL editor of Xilinx ISE 14.1 EDA (Electronic Design Automation) tool. Behavioural simulation is done to check the design logic and functionality, using Xilinx ISE simulatorAfter that, the design is put into practice using FPGA to confirm that the Intelligent Router operates as intended. The Data featurization will lessen the networks' redundancy [21-23].

A. Simulation Results for Accurate Time-based generator

Practically generating low frequencies like 1 Hz /10Hz accurately is tough. Normal strategy will be to have a stable high frequency above 1 MHz and then successfully divide it several times using decade counter, sending TC as ripple clock input.

In the proposed router architecture design, an FPGA onboard clock of 10MHz is divided 7 times using 7-decade counters to obtain 1 Hz or 1-second pulse as shown in Fig.11 and this 1 Hz or 1-sec pulse will be used as input to SDCR clock input in proposed Intelligent Router based on data rates. The Accurate Time-based Generator (ATG) output for varied frequency is shown from Fig.12-14.

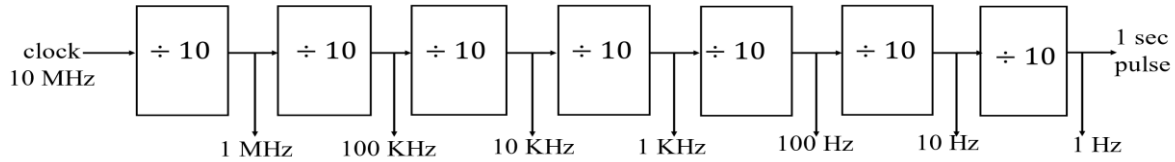


Fig. 11 Accurate Time-based Generator (ATG) to frequency scale down the clock from 10MHz to 1Hz

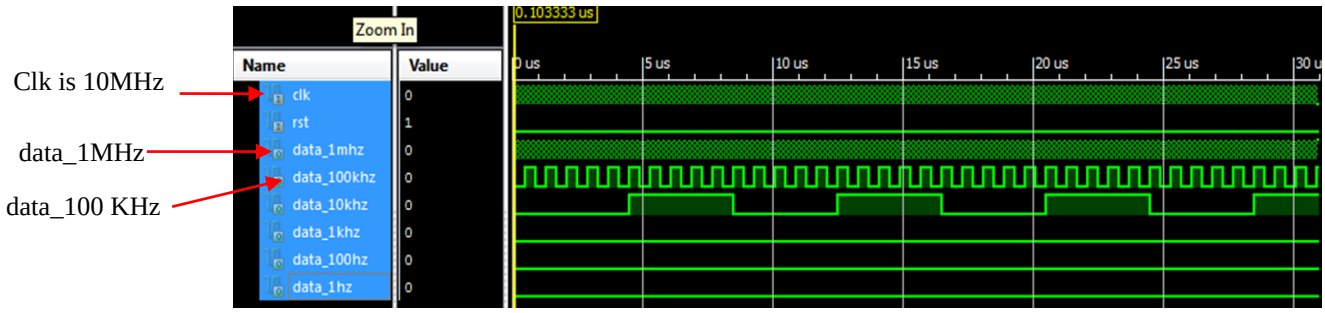


Fig. 12. Simulation waveform of ATG generating the 1 MHz and 100KHz divided from 10MHz clock

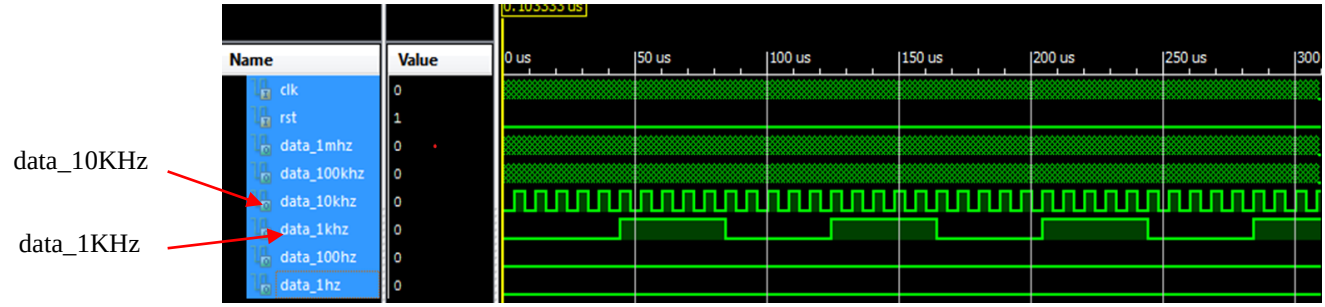


Fig. 13. Simulation waveform of ATG generating the 10KHz and 1KHz signal clock

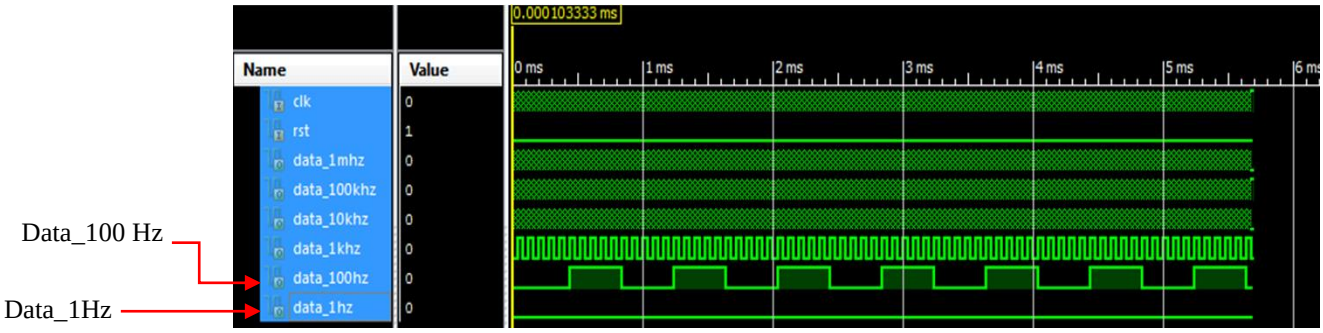


Fig. 14. Simulation waveform of ATG generating the 100Hz, 1Hz signal clock

B. Simulation Results of DRIR

The simulation results for data rate-based routing is shown in Fig. 15. i_data is the continuous data that enters the router (DRIR). Here threshold value set for testing the device is '4' in binary "0100". Clock of 10 MHz is applied. When reset signal is received goes from high to low, the router is enabled. The on_count signal is initialized to zero and will be incremented gradually as and when the data is received. When the on_count_reg ≤ "i_ref = 4", data is low duration pulse which indicates that they are high-frequency data. This data is then directed to high-frequency output-line o_high_frq during o_high_valid = '1' from 130 ns to 300 ns. The data's rate and the frequency are directly proportional to each other. Data Rate = 2 x operating frequency. Similarly, when on_count_reg ≥ i_ref, the data is high duration pulse, whose data rate is low as seen on o_low_frq output line during o_low_ valid = 1 from 310 ns to 1010 ns. This methodology of routing the data continues as there is continuous data hitting the router.

C. Simulation Results of DDIR

Simulation Results for Data Duration-based Intelligent Router design is shown in Fig. 17. The data is carried by a free running clock of 10MHz, which is split by the ATG into a 1 Hz clock. i_data is the data input which is shown as persistent and continuous data. Frequency of clock exceeds that of the data. Reset is assigned at the 1st clock cycle. As indicated in Table II, data present between 0 to 5 clock pulses, will be sent to SDDR. Hence Data enters MDDR after SDDR is tri-stated when the count value is 6. The data is exclusively sent through MDDR between 6 and 9. Data is sent through LDDR and MDDR is tri-stated after the count hits nine. In the Fig. 16 SDDR, MDRR and LDDR is channelized from output line o_short_data, o_medium_data, o_long_data resprctively. The first five pulses of the data will be short duration, lasting 20 to 110 ns. After that, the data will be routed to a medium duration line, lasting 110 to 190 ns, as long as the data pulse remains on i_data until the medium_duration register count hits 10. If the data persists beyond medium duration of 10 then the rest data will be routed on to long duration data line from 190 ns onwards and it persists till the long_duration_count is 20. This reference duration taken is for user ease. For user convenience, this reference duration has been taken. The network administrator has real-time access to track data and establish reference values. LDDR is used to route the data until it is reset again. The preceding cycle of data-routing via SDDR, MDDR, and LDDR repeats once a reset is performed. Hence duration-based data-segregation continues as data the live-data hits the intelligent router.

D.Simulation Results for DSIR

Simulation Results for Data Size-dependent Fig. 17 depicts an intelligent router design. Here, the clock runs asynchronously (free). At the first-clock-edge, reset (i_rst) is applied. i_data hits after 3-clock cycles. The threshold set is 4-bytes, input-data is handled like regular data from 90 to 130 ns once data_count = 3 and reference_count = 4. The Bulk data threshold can be set as per data situation and it is user programmable. From 240 to 300 ns data_count ≥ reference_count, the i_data is dealt as bulk data. After the input data-count value reaches 5, data is shifted from normal path to bulk data path. Suitable line buffers are used to collect Normal and Bulk Data to avoid retransmission.

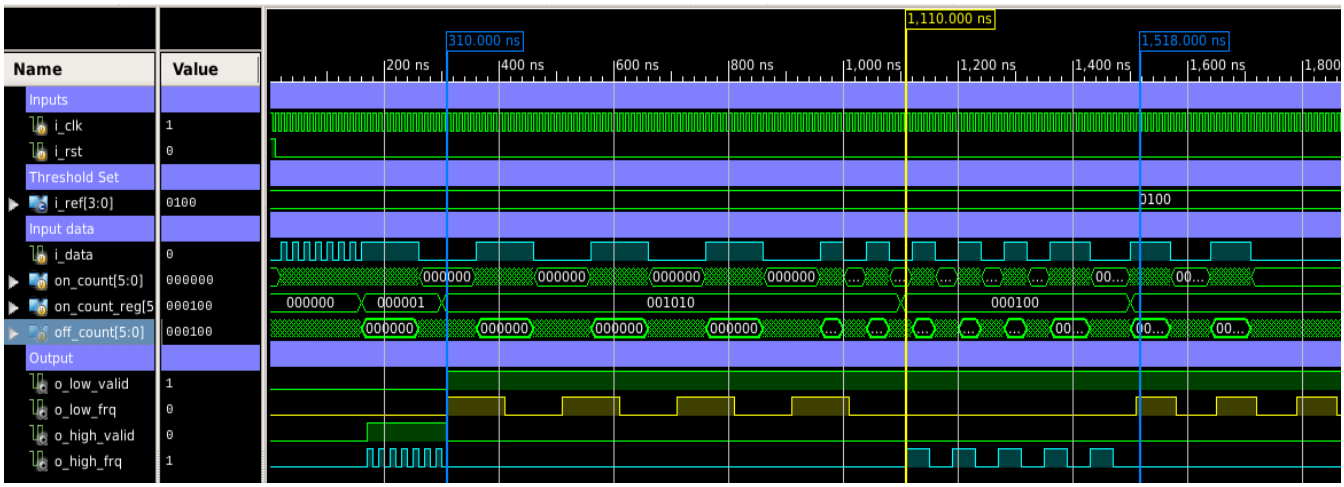


Fig. 15 Simulation Waveform depicting data segregation as low data rate and high data rate by DRIR

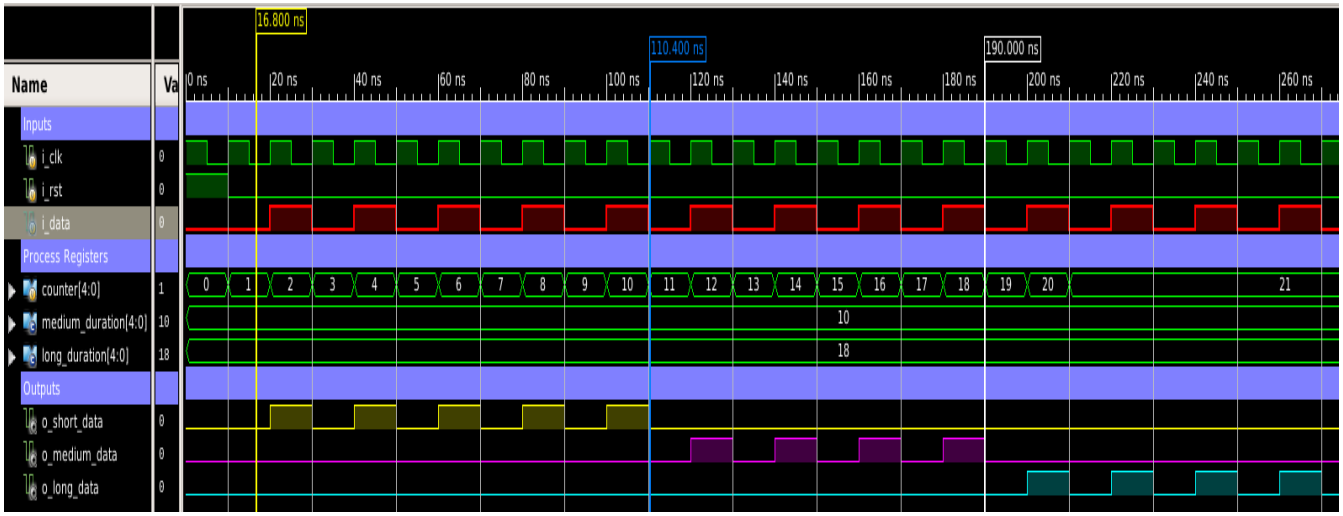


Fig. 16. Simulation waveform depicting data segregation as short, medium, and long data duration by DDIR

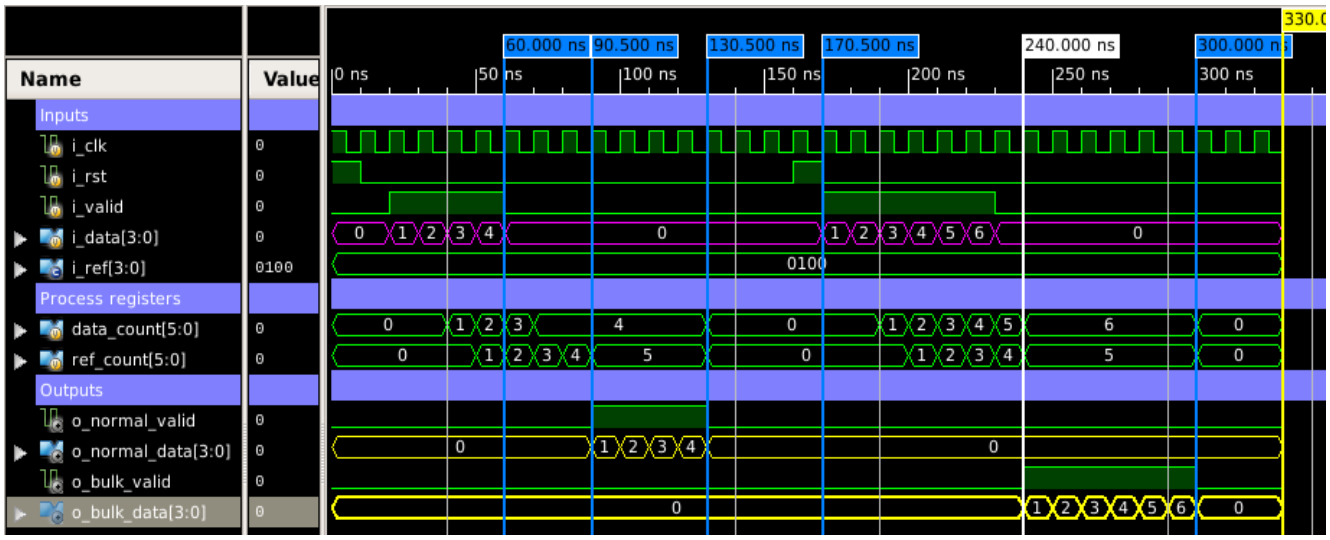


Fig. 17. Simulation waveform depicting data segregation as normal and bulk data by DSIR

TABLE III
DEVICE UTILIZATION SUMMARY

Logic Utilization	Data Rate Router			Data Duration Router		Data Size Router	
	Available	Used	Utilization %	Used	Utilization %	Used	Utilization %
Slice of Flip Flops	7168	92	1%	8	1%	427	5%
4 input LUTs	7168	105	1%	13	1%	423	5%
Occupied Slices	3584	90	2%	10	1%	423	11%
Slices containing only related logic	-	90	100%	10	100%	423	100%
Slices containing unrelated logic	90	0	0%	0	0%	0	0%
Logic	-	104	-	-	-	345	-
Shift registers	-	1	-	-	-	78	-
Bonded IOBs	141	7	4%	6	4%	17	12%
BUFGMUXs	8	1	12%	1	12%	2	25%
Average Fanout of Non-Clock Nets	-	3.67	-	3.33	-	3.30	-

E. Design Outcome

Intelligent Router Verilog-code is edited in HDL-editor of Xilinx ISE 14.1 EDA (Electronic Design Automation) tool. The design is programmed on FPGA (xc3s400pq208-4) to test the functionality and get performance features of the Intelligent Router as per the expected design. Analyzing the data and its reasonable fusion with the network structure information is handled. The Data featurization will reduce the redundancy in the network. The results of proposed router are Xilinx ISE 14.7 PAR estimation for the FPGA.

TABLE IV
TIMING REPORTS OF PROPOSED INTELLIGENT ROUTERS

Data Size Router Run-time	Data Duration Router Run-time	Data Rate Router Run-time
10.851 ns	10.915 ns	5.798 ns

TABLE V
POWER REPORT OF PROPOSED INTELLIGENT ROUTERS

Router	Static Power (mW)	Dynamic Power(mW)	Total Power(mW)
Data Size Router	60	NIL	60
Data Duration Router	61.05	2.45	63
Data Rate Router	65	NIL	65

Device Utilization Summary, Device Timing report and Power estimation of the proposed Intelligent Routers DRIR, DDIR and DRIR are tabulated in Table III and Table IV and Table V respectively. The internal clock to set remains the same for all the router modules. As the device used has large number of logical cells the module occupies very less percentage of LUT's.

If smaller FPGAs are used then proposed router device utilization be significantly improved. Data Rate of the proposed router is calculated as 344.9 Mbps

Data Rate = 2 x operating frequency
= 2 x (1/ Best case Run-time)
= 2 x (1 / 5.798 ns)
= 344.9 Mbps

For the Intelligent Router at worst case of run time is 10.915 ns for which the data rate is 183.23 Mbps

F. Proposed Design Performance Comparison

Power Comparison

Power used by proposed Intelligent Router ranges from 60mW to 65 mW under ambient temperature of 82.7^0C, Effective TJA of 35.2^0C/W, Junction Temperature is 27.3^0C. in the proposed work done.

TABLE VI
POWER ESTIMATION COMPARISON

Router	Static Power (mW)
NeuronLink	648
Reconfigurable NOC	1000
SbRN NOC Based Router	456
Proposed Intelligent Router based on Data Rate	65
Proposed Intelligent Router based on data Size	60
Proposed Intelligent Router Based on Data Duration	63

It is observed that proposed router consumes less power compared to SbRN algorithm-based NOC Router[22], NeuronLink[23] and Reconfigurable NoC[24] as shown in Fig. 18 and Table VI.

The run time is in nano seconds (10.915 ns) where hybrid or cloud-based routers takes 5 milliseconds to ping on high-speed network tested by OOKLA web-based internet speed measuring application [29]. The graphical representation of this comparison is shown in Fig. 18. Power estimation is very important in digital design as it directly affects the battery life.

Data Rate Comparison

There are various software routing algorithms available like Adhoc On-demand Distance Vector Routing (AODV)[25], Routing Information Protocol (RIP)[26], Open Shortest Path First (OSPF)[26] are few among them. When compared with the proposed Intelligent Router, proposed router data rate is 275.14 Mbps which is extremely better. The graphical representation of this comparison is shown in Fig. 19.

TABLE VII
DATA RATE COMPARISON

Routing Techniques	Data Rate in Mbps
AODV	2.5
TC-AODV	2.5
RIPV2 in CISCO using IPV4 best case	96
RIPV2 in Vyatta using IPV4 best case	31
OSPFV2 in CISCO using IPV4 best case	74
OSPFV2 in Vyatta using IPV4 best case	35
Proposed Intelligent Router	275.14

Run Time Comparison

When compared with other software algorithm-based routing technique[8], [25-27] as listed in Table VIII, the proposed Intelligent Router at best case shows 9-times speedup. The run time of the proposed router calculated is 10,915 ns at the last extreme output port of FPGA. The graphical representation of this comparison is shown in Fig. 20.

TABLE VIII
RUN TIME COMPARISON

Routing Techniques	Run Time in ms
Bellman ford	513
Bellman ford with dragonfly	0.1
SSP_EP, SSP_VP	0.1
Eager Dijkstra	0.1
AODV Malicious Node attack	14
TC-AODV	18
RIPV2 in CISCO	68
RIPV2 in Vyatta	69
OSPFV2 in CISCO	48
OSPF in Vyatta	62
Proposed Intelligent Router	0.000010915 (10.915 ns)

Operating Frequency Comparison

Operating frequency achieved by the Intelligent Router is 137.57 MHz which when compared to other routing techniques is less but as frequency is above 100 MHz, Intelligent Router can handle easy transmission of 4K Live Video Streaming[28] as shown in table IX. This can be improved by Logic optimization in future. The graphical representation of this comparison is shown in Fig. 21.

TABLE IX
OPERATING COMPARISON

Router	Operating Frequency in MHz
Stall	195
Skid Buffer	299
Min-Area Skid Buffer	301
Neuron Link	300
Reconfigurable NoC	350
Proposed Intelligent Router	137.57

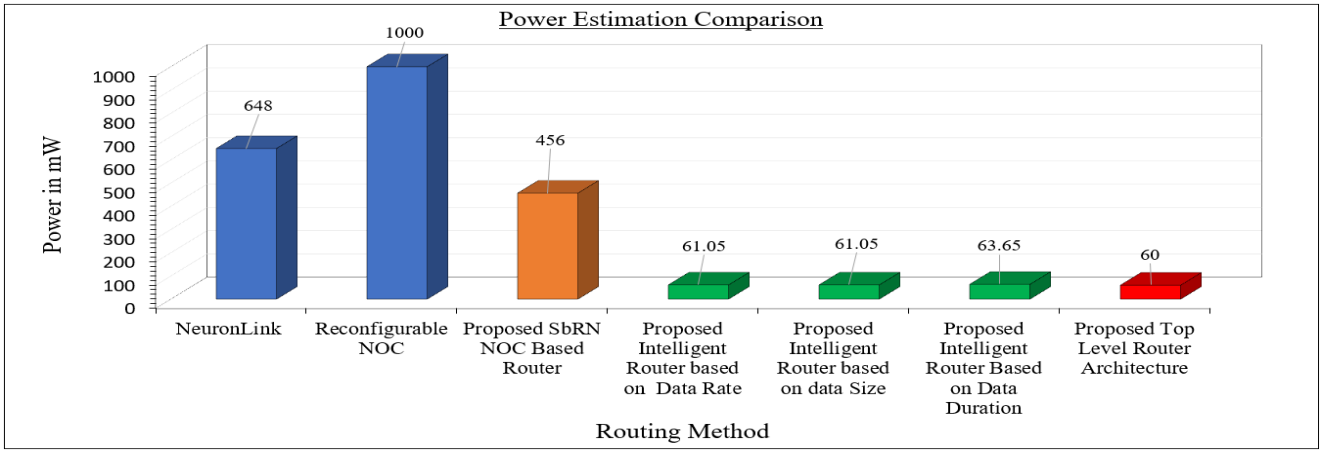


Fig. 18 Power Estimation Comparison

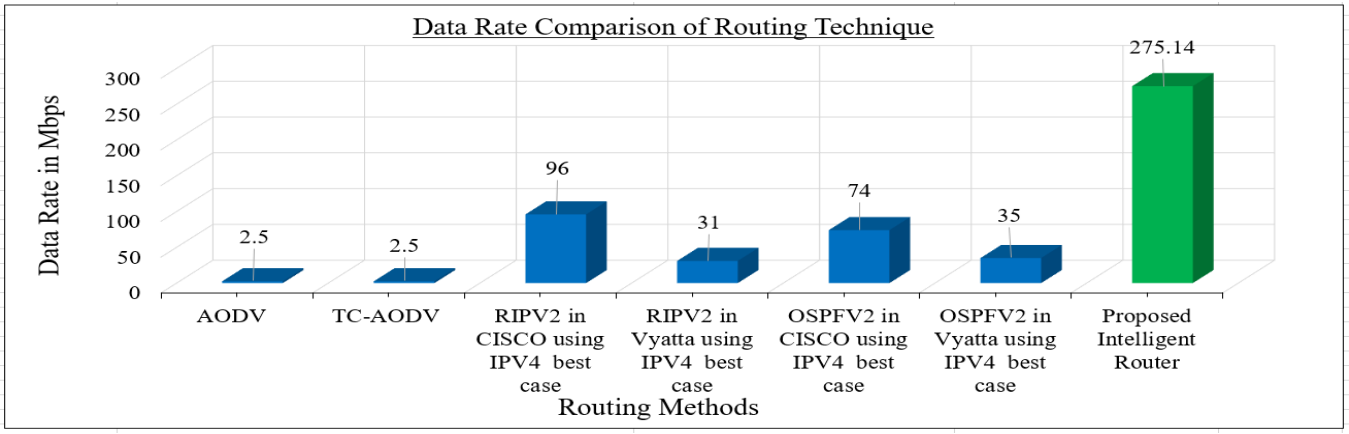


Fig. 19 Data Rate Comparison

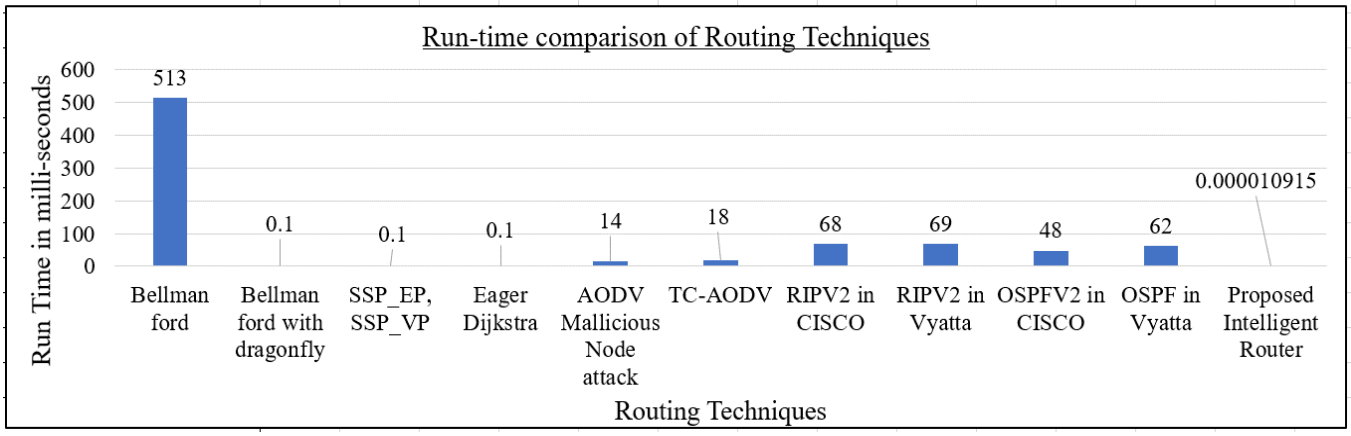


Fig. 20 Run-Time Comparison

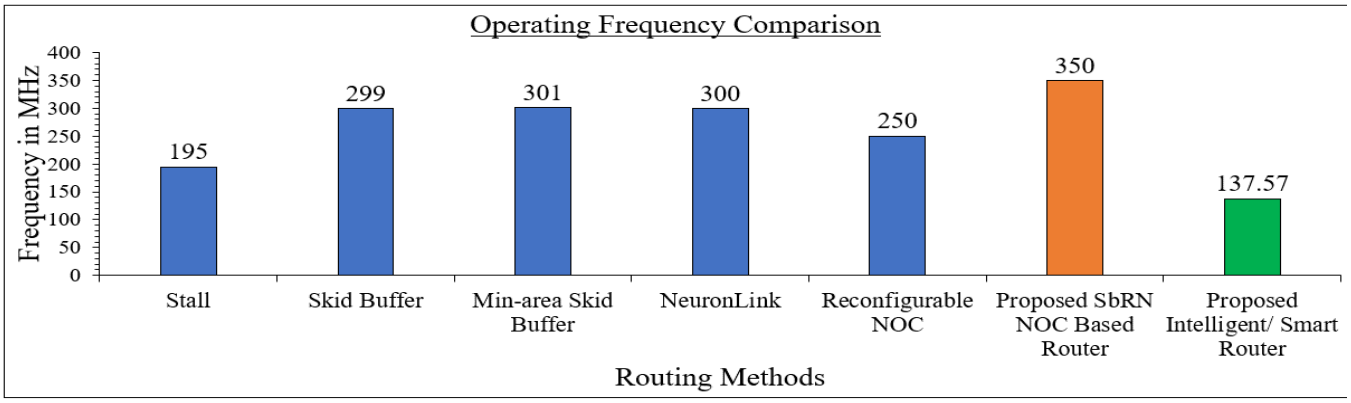


Fig. 21 Operating Frequency Comparison

V. Conclusion

In this paper three designs on Intelligent routing techniques that use size, rate and duration-based data segregation is experimented. For dynamic routing applications, this approach is important. With the use of Verilog HDL, Xilinx Simulator was used to program and simulate the digital design process for all the three Intelligent Routing Techniques proposed. FPGA Spartan-3 XC3s400pQ208-5 was used for implementation. This experiment is a submodule of top-level Router Architecture which is ongoing research.

In this proposed work we claim that the speed and performance is better than the algorithm-based routers as there is no CPU utilization by the router for data transfer. The critical path delay is recorded as 10.915 ns at the worst case. Hence the operating frequency would be 137.57 MHz with a data rate of 275 Mbps. Power utilization is 85.7 to 89.9% reduced compared to Reconfigurable NOC and Strawberry based Recurrent Network (SbRN) NOC Router.

The proposed Intelligent Router can be placed anywhere in the network hierarchy, either at the exchange or in edge routers, depending on usage, to reduce the complexity in data monitoring while routing. It can be used with many data dissemination techniques. In the best-case scenario, post restriction, FPGA speed grade, and WiFi could limit the router's capability. The proposed study is a design approach that routes data intelligently using data properties, without design optimization processes of the tool. In future, more study on logic and design optimization may be done.

References

[1] C. Chen, L. Liu, T. Qiu, D. O. Wu, and Z. Ren, "Delay-Aware Grid-Based Geographic Routing in Urban VANETs: A Backbone Approach," *IEEE/ACM Transactions on Networking*, vol. 27, no. 6, pp2324–2337, 2019, doi: 10.1109/TNET.2019.2944595

[2] Z. Tian, S. Su, W. Shi, X. Du, M. Guizani, and X. Yu, "A data-driven method for future Internet route decision modeling," *Future Gener. Comput. Syst.*, vol. 95, pp212–220, 2019, https://doi.org/10.1016/j.future.2018.12.054

[3] Kashif Naseer Qureshi, Francesco Piccialli, Gwanggil Jeon, and Sadia Din, "Link quality and energy utilization based preferable next hop selection routing for wireless body area networks," *Computer Communications*, vol. 149, pp382–392, 2020, doi: https://doi.org/10.1016/j.comcom.2019.10.030

[4] T. Patil and A. Sandi, "Design and implementation of asynchronous NOC architecture with buffer-less router," *Materials Today: Proceedings*, vol. 49, pp756–763, 2022, doi: https://doi.org/10.1016/j.matpr.2021.05.282

[5] K. Haseeb, N. Islam, T. Saba, A. Rehman, and Z. Mehmood, "LSDAR: A light-weight structure-based data aggregation routing protocol with secure internet of things integrated next-generation sensor networks," *Sustainable Cities and Society*, vol. 54, pp101995, 2020, https://doi.org/10.1016/j.scs.2019.101995

[6] F. Fanian and M. K. Rafsanjani, "Cluster-based routing protocols in wireless sensor networks: A survey based on methodology," *Journal of Network and Computer Applications*, vol. 142, pp111–142, 2019, doi: https://doi.org/10.1016/j.jnca.2019.04.021

[7] I. Rasheed, F. Hu, Y.-K. Hong, and B. Balasubramanian, "Intelligent Vehicle Network Routing with Adaptive 3D Beam Alignment for mmWave 5G-Based V2X Communications," *IEEE Transactions on Intelligent Transportation Systems*, vol. 22, no. 5, pp2706–2718, 2021, doi: 10.1109/TITS.2020.2973859

[8] Z. Khan, P. Fan, F. Abbas, H. Chen, and S. Fang, "Two-Level Cluster Based Routing Scheme for 5G V2X Communication," *IEEE Access*, vol. 7, pp16194–16205, 2019, doi: 10.1109/ACCESS.2019.2892180

[9] Y. Kang, X. Wang, and Z. Lan, "Study of Workload Interference with Intelligent Routing on Dragonfly," in *SC22: International Conference for High Performance Computing, Networking, Storage and Analysis*, 2022, pp1–14. doi: 10.1109/SC41404.2022.00025

[10] S. K. Lakshmanaprabu et al., "An effect of big data technology with ant colony optimization-based routing in vehicular ad hoc networks: Towards smart cities," Journal of Cleaner Production, vol. 217, pp584-593, 2019, doi: https://doi.org/10.1016/j.jclepro.2019.01.115

[11] M. L. V. C. Aswini, "Artificial Intelligence Based Smart Routing in Software Defined Networks," *Computer Systems Science and Engineering*, vol. 44, no. 2, pp1279–1293, 2023, doi: 10.32604/csse.2023.022023

[12] D. Zhang, T. Zhang, and X. Liu, "Novel self-adaptive routing service algorithm for application in VANET," *Applied Intelligence*, vol. 49, no. 5, pp1866–1879, May 2019, doi: 10.1007/s10489-018-1368-y

[13] J. Fang, Z. Chang, and D. Li, "Exploration on Routing Configuration of HNoC With Intelligent On-Chip Resource Management," *IEEE Access*, vol. 8, pp12117–12129, 2020, doi: 10.1109/ACCESS.2019.2958945

[14] W. Sun, S. Yue, Q. Liu, X. Lin, and W. Hu, "Bulk Data Transfer with Store-and-Forward in Wide Area Networks," *2019 21st International Conference on Transparent Optical Networks (ICTON)*, pp1–4, 2019, doi: 10.1109/ICTON.2019.8840553

[15] P. Sarao, "Data Rate Based Route Evaluation in MANET,"," *2021 5th International Conference on Electronics, Communication and Aerospace Technology (ICECA), Coimbatore, India*, pp563–569, 2021, doi: 10.1109/ICECA52323.2021.9675903

[16] J. Wu, J. Zhang, Z. Han, L. F. Liu, and J. Dong, "The Implementation of a High-Speed Ethernet Traffic Generator Based on FPGA," in *Materials Science and Information Technology*, in Advanced Materials Research, vol. 433. Trans Tech Publications Ltd, Feb. 2012, pp7530–7534, doi: 10.4028/www.scientific.net/AMR.433-440.7530

[17] J. Henaut, D. Dragomirescu and R. Plana, "FPGA Based High Date Rate Radio Interfaces for Aerospace Wireless Sensor Systems," *2009 Fourth International Conference on Systems*, pp173-178, 2009, doi: 10.1109/ICONS.2009.28

[18] Yongzhi Liao, and Qilin Tang, "Multiple Periodic Solutions for Cohen-Grossberg BAM Neural Networks with Mixed Delays and Impulses," Engineering Letters, vol. 30, no.4, pp1185-1198, 2022

[19] Chenze Huang and Ying Zhong, "A Network Representation Learning Method Fusing Multi-Dimensional Classification Information of Nodes," IAENG International Journal of Computer Science, vol. 50, no. 1, pp94–105, 2023

[20] Bimal Chandra Das, Md. Waliur Rahman Miah, Narayan Ranjan Chakraborty, Md. Samzid Bin Hafiz, and Momotaz Begum, "Green Hose-Rectangle Model Approach for Power Efficient Communication Networks," IAENG International Journal of Computer Science, vol. 48, no. 3, pp760–769, 2021

[21] Qingrong Wang, Kai Zhang, Changfeng Zhu, and Yutong Zhou, "A Multi-regional Spatio-temporal Network for Traffic Accident Risk Prediction," Engineering Letters, vol. 31, no. 3, pp906–918, 2023

[22] Sumana Achar and Jayadevappa D, "Optimized Recurrent based Training Accelerator for Network-On-Chip Communication System," IAENG International Journal of Computer Science, vol. 50, no. 4, pp1410–1419, 2023

[23] Xiao and Shanlin, et al., "NeuronLink: An Efficient Chip-to-Chip Interconnect for Large-Scale Neural Network Accelerators," IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 28, no. 9, pp1966–1978, 2020

[24] M. Oveis-Gharan and G. N. Khan, "Reconfigurable on-chip interconnection networks for high performance embedded SoC design," Journal of Systems Architecture, vol. 106, pp101711, 2020, doi: https://doi.org/10.1016/j.sysarc.2020.101711

[25] S. Li and B. Gong, "Developing a reliable route protocol for mobile self-organization networks," High-Confidence Computing, vol. 4, no. 3, pp100194, 2024, doi: https://doi.org/10.1016/j.hcc.2023.100194

[26] Edward Guillen, Ana María Sossa and Edith Paola Estupinan, "Performance Analysis over Software Router vs. Hardware Router: A Practical Approach", Lecture Notes in Engineering and Computer Science: Proceedings of The World Congress on Engineering and Computer Science 2012, WCECS 2012, 24-26 October, 2012, San Francisco, USA, pp973-978.

[27] S. W. G. AbuSalim, R. Ibrahim, M. Z. Saringat, S. Jamel, and J. A. Wahab, "Comparative Analysis between Dijkstra and Bellman-Ford Algorithms in Shortest Path Optimization," IOP Conference Series: *Materials Science and Engineering*, vol. 917, no. 1, pp012077, 2020, doi: 10.1088/1757-899X/917/1/012077

[28] "Building Home Networks with High-Quality 4K Video Experience", *HUAWEI Technical White Paper on the SmartWi-Fi 4K Video Transmission Solution*

[29] "OOKLA Speed Test", (accessed August 08, 2024), https://www.speedtest.net/result/16596259460

Sumana Achar born in Ambikanagar, Uttara Kannada District of Karnataka, India in 2nd July 1980. She is a Research Scholar at JSS Academy of Technical Education, Bengaluru and has received M.Tech. degree in VLSI Design and Embedded Systems from BVB College of Engineering, Hubli, Karnataka, India in 2009. Her major field of study is VLSI Design and Embedded Systems. She has 18 years of experience in teaching at Engineering Institutions and 2 years of Industrial Experience. Her current research interest is networking. Ms. Achar is the member of IAENG, ISTE.

D. Jayadevappa is the member of IAENG since 2008. He was born in Kabbur, Karnataka, India in 1970. He holds a Ph.D. degree from JNTU college of Engineering, Kakinada, Andhra Pradesh., India, M.Tech. degree from SJCE, Mysore, VTU, in 2000 with specialization in Bio-Medical Instrumentation. He received his B.E. degree in Instrumentation Technology from SIT, Tumkur, Bangalore University in 1994. He is currently Professor and Principal of Dr. H.N. National College of Engineering, Bengaluru, Karnataka, India. He has 28 years of teaching and industrial experience and is the Member of IAENG, IETE, ISTE & BMESI. He has published more than 120 papers in International Journals and conferences. Two papers published in IAENG-IJCS. His areas of interests are Digital Image Processing, Bio-Medical Signal Processing and Networking.